ESP32-PICO-V3-ZERO

Datasheet

Alexa Connect Kit (ACK) module with an Espressif chipset
2.4 GHz Wi-Fi + Bluetooth® + Bluetooth LE support
Built around ESP32 series of SiP, Xtensa® dual-core 32-bit LX6 microprocessor
4 MB flash available
On-board PCB antenna with an RF test connector

ESP32-PICO-V3-ZERO

Version 1.4
Espressif Systems

1 Module Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/sites/default/files/documentation/esp32-pico-v3-zero_datasheet_en.pdf

1.1 Features

CPU and On-Chip Memory

- ESP32 embedded, Xtensa dual-core 32-bit LX6 microprocessor, up to 240 MHz
- 448 KB ROM
- 520 KB SRAM
- 16 KB SRAM in RTC

Wi-Fi

- 802.11b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel: 2412 ~ 2484 MHz

Bluetooth

- Bluetooth V4.2 BR/EDR and Bluetooth LE specification
- Class-1, class-2 and class-3 transmitter
- AFH
- CVSD and SBC

Peripherals

- 2 × UART (one for connection to the host and the other for debugging), EN pin, and interrupt pin

Integrated Components on Module

- 40 MHz crystal oscillator
- 4 MB SPI flash

Antenna Options

- On board PCB antenna with an RF test connector

  Note:
  This connector is for test only, and must not be used for connecting an external antenna.

Operating Conditions

- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating temperature range: –40 ~ 85 °C

Certification

- Bluetooth certification: BQB (ID: D050108)
- RF certification: See Certification
- Green certification: REACH/RoHS

1.2 Description

The ESP32-PICO-V3-ZERO is a module that is based on ESP32-PICO-V3, a System-in-Package (SiP) device. It provides complete Wi-Fi and Bluetooth functionalities with embedded Xtensa dual-core 32-bit LX6 microprocessor. The module integrates a 4 MB SPI flash.

At the core of this module is the ESP32 chip, which is a single 2.4 GHz Wi-Fi and Bluetooth combo chip designed with TSMC's 40 nm low-power technology. ESP32-PICO-V3-ZERO integrates all peripheral components seamlessly, including a crystal oscillator, flash, filter capacitors and RF matching links in one single

package. Module assembly and testing are already done at SiP level. As such, ESP32-PICO-V3-ZERO reduces the complexity of supply chain and improves control efficiency. It is ultra-small in size, with robust performance and low energy consumption.

ESP32-PICO-V3-ZERO is a module for Alexa Connect Kit (ACK), a managed service that makes it easy to integrate Alexa into your products. With ESP32-PICO-V3-ZERO and its default firmware, you can connect your devices or system to Alexa and the Internet without worrying about managing cloud services, writing an Alexa Skill, or developing complex networking and security firmware. If you add ESP32-PICO-V3-ZERO to your device, you can easily, quickly and economically create products that customers love.

Note:

- For more information on ESP32, please refer to *ESP32 Series Datasheet*.
- For more information on ESP32-PICO-V3, please refer to *ESP32-PICO-V3 Datasheet*.

Contents

1 Module Overview 2
1.1 Features 2
1.2 Description 2
2 Block Diagram 8
3 Pin Definitions 9
3.1 Pin Layout 9
3.2 Pin Description 10
3.3 Strapping Pins 10
4 Electrical Characteristics 13
4.1 Absolute Maximum Ratings 13
4.2 Recommended Operating Conditions 13
4.3 DC Characteristics (3.3 V, 25 °C) 13
4.4 Current Consumption Characteristics 14
4.5 Wi-Fi RF Characteristics 15
4.5.1 Wi-Fi RF Standards 15
4.5.2 Transmitter Characteristics 15
4.5.3 Receiver Characteristics 16
4.6 Bluetooth Radio 17
4.6.1 Receiver – Basic Data Rate 17
4.6.2 Transmitter – Basic Data Rate 18
4.6.3 Receiver – Enhanced Data Rate 18
4.6.4 Transmitter – Enhanced Data Rate 19
4.7 Bluetooth LE Radio 19
4.7.1 Receiver 19
4.7.2 Transmitter 20
5 Peripheral Schematics 21
6 Physical Dimensions and PCB Land Pattern 22
6.1 Physical Dimensions 22
6.2 PCB Layout 23
6.2.1 Recommended PCB Land Pattern 23
6.2.2 PCB Layout Guide 24
6.3 Dimensions of RF Test Connector 26
7 Product Handling 27
7.1 Storage Conditions 27
7.2 Electrostatic Discharge (ESD) 27
7.3 Reflow Profile 27
7.4 Ultrasonic Vibration 28

8 Related Documentation and Resources 29

Revision History 30

List of Tables

1 Pin Definitions 10
2 Strapping Pins 11
3 Parameter Descriptions of Setup and Hold Times for the Strapping Pins 12
4 Absolute Maximum Ratings 13
5 Recommended Operating Conditions 13
6 DC Characteristics (3.3 V, 25 °C) 13
7 Current Consumption Depending on RF Modes 14
8 Current Consumption Depending on Work Modes 15
9 Wi-Fi RF Standards 15
10 TX Power Characteristics 16
11 RX Sensitivity Characteristics 16
12 RX Maximum Input Level 17
13 Adjacent Channel Rejection 17
14 Receiver Characteristics – Basic Data Rate 17
15 Transmitter Characteristics – Basic Data Rate 18
16 Receiver Characteristics – Enhanced Data Rate 18
17 Transmitter Characteristics – Enhanced Data Rate 19
18 Receiver Characteristics – Bluetooth LE 20
19 Transmitter Characteristics – Bluetooth LE 20

List of Figures

1 ESP32-PICO-V3-ZERO Block Diagram 8
2 Pin Layout (Top View) 9
3 Setup and Hold Times for the Strapping Pins 12
4 Peripheral Schematics 21
5 Physical Dimensions 22
6 Recommended PCB Land Pattern 23
7 Module Placement on a Base Board 25
8 Keepout Zone for Module's Antenna on the Base Board 25
9 Dimensions of RF Test Connector 26
10 Reflow Profile 27

2 Block Diagram

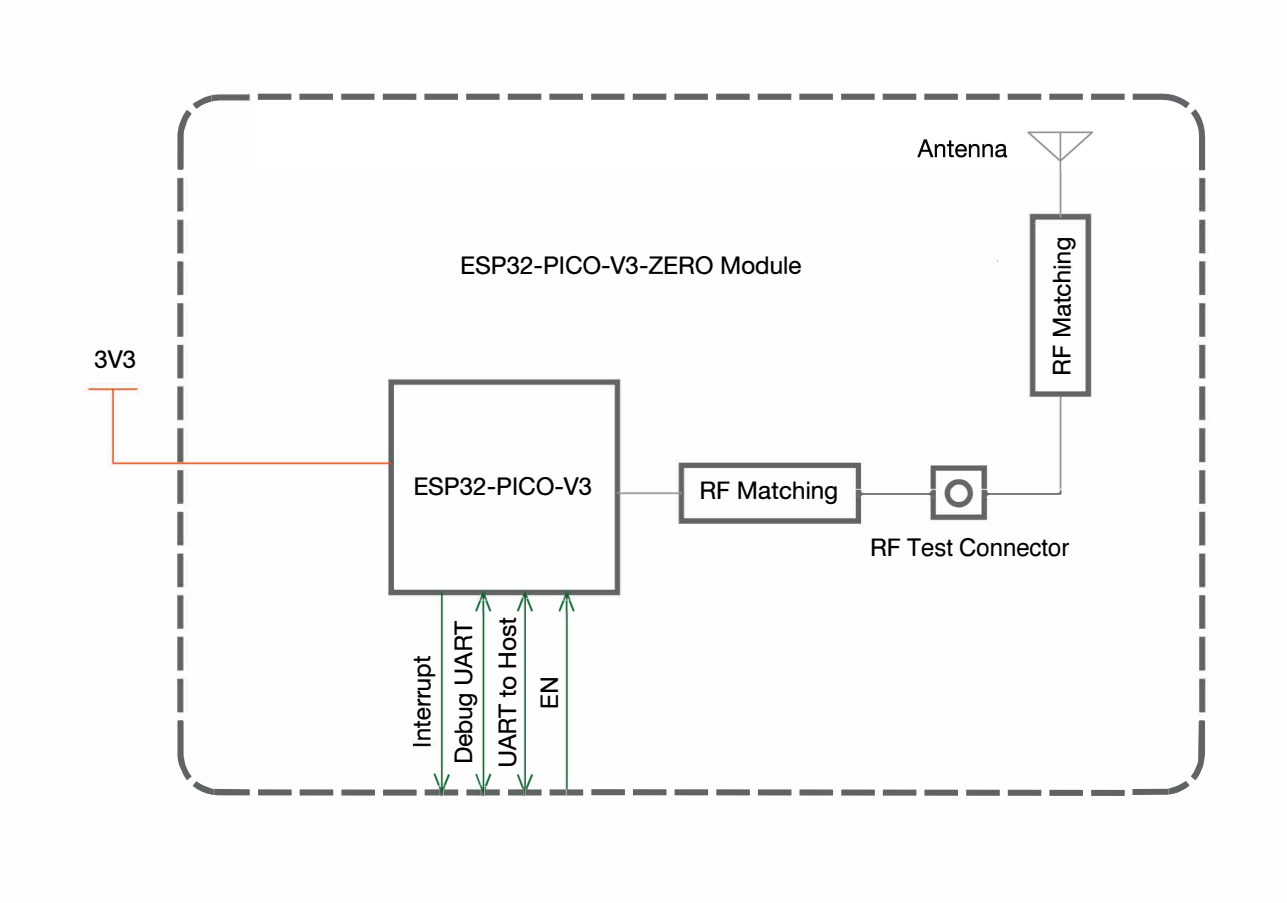

Figure 1: ESP32-PICO-V3-ZERO Block Diagram

3 Pin Definitions

3.1 Pin Layout

The pin diagram below shows the approximate location of pins on the module. For the actual diagram drawn to scale, please refer to Figure 6.1 *Physical Dimensions*.

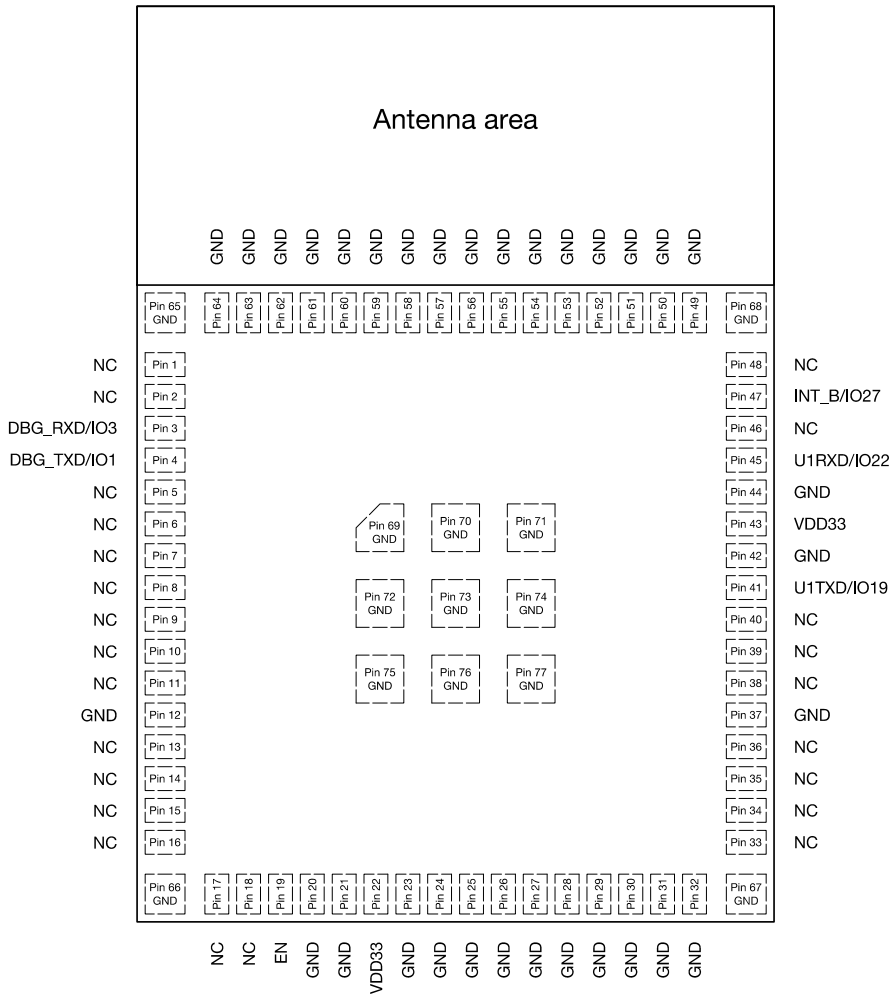

Figure 2: Pin Layout (Top View)

3.2 Pin Description

The module has 77 pins. See pin definitions in Table 1.

For peripheral pin configurations, please refer to *ESP32 Series Datasheet*.

Table 1: Pin Definitions

Name	No.	Type[1]	Function
NC	1, 2, 5 ~ 11, 13 ~ 18, 33 ~ 36, 38 ~ 40, 46, 48	NA	Do not connect. These pins must be left floating.
DBG_RXD/IO3	3	I	GPIO3, Debugging UART RX, GPIO3
DBG_TXD/IO1	4	O	GPIO1, Debugging UART TX, GPIO1
EN	19	I	High: On; enables the module Low: Off; the module powers off Note: Do not leave this pin floating.
VDD33	22	P	Power supply (3.0 V ~ 3.6 V)
U1TXD/IO19	41	O	UART TX, connected to host RX, GPIO19
VDD33	43	P	Power supply (3.0 V ~ 3.6 V)
U1RXD/IO22	45	I	UART RX, connected to host TX, GPIO22
INT_B/IO27	47	O	Host interrupt, connected to host GPIO, GPIO27
GND	12, 20, 21, 23 ~ 32, 37, 42, 44, 49 ~ 77	P	Ground

[1] P: power supply; I: input; O: output.

[2] IO7/IO8/IO9/IO10/IO20 belong to VDD_SDIO power domain and can not work when VDD_SDIO power shuts down.

3.3 Strapping Pins

Note:
The content below is excerpted from Section Strapping Pins in *ESP32 Series Datasheet*.

ESP32 has five strapping pins:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 2 for a detailed boot-mode configuration by strapping pins.

Table 2: Strapping Pins

Voltage of Internal LDO (VDD_SDIO)					
Pin	Default	3.3 V		1.8 V	
MTDI	Pull-down	0		1	
Booting Mode					
Pin	Default	SPI Boot		Download Boot	
GPIO0	Pull-up	1		0	
GPIO2	Pull-down	Don't-care		0	
Enabling/Disabling Debugging Log Print over U0TXD During Booting					
Pin	Default	U0TXD Active		U0TXD Silent	
MTDO	Pull-up	1		0	
Timing of SDIO Slave					
Pin	Default	FE Sampling FE Output	FE Sampling RE Output	RE Sampling FE Output	RE Sampling RE Output
MTDO	Pull-up	0	0	1	1
GPIO5	Pull-up	0	1	0	1

* FE: falling-edge, RE: rising-edge
* Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave", after booting.
* The module integrates a 3.3 V SPI flash, so the pin MTDI cannot be set to 1 when the module is powered up.

The illustration below shows the setup and hold times for the strapping pins before and after the CHIP_PU signal goes high. Details about the parameters are listed in Table 3.

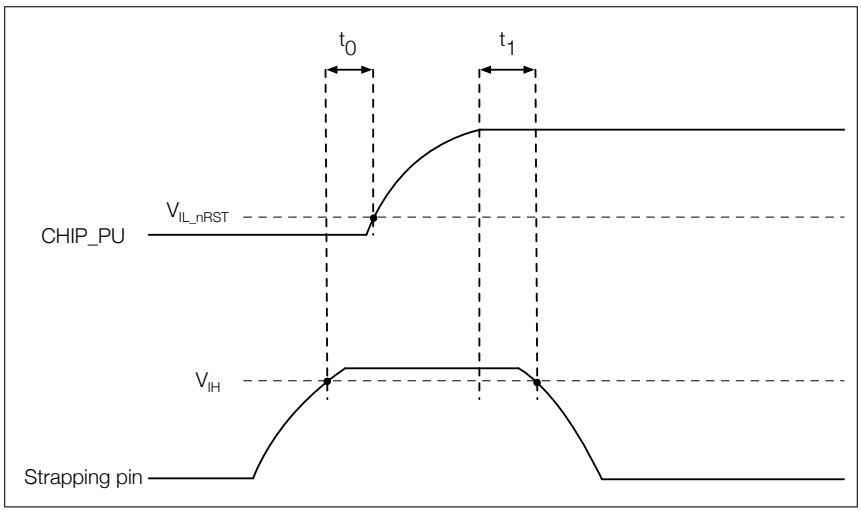

Figure 3: Setup and Hold Times for the Strapping Pins

Table 3: Parameter Descriptions of Setup and Hold Times for the Strapping Pins

Parameters	Description	Min.	Unit
t_0	Setup time before CHIP_PU goes from low to high	0	ms
t_1	Hold time after CHIP_PU goes high	1	ms

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses above those listed in *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	85	°C

* Please see Appendix IO MUX of *ESP32 Series Datasheet* for IO's power domain.

4.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
I_{VDD}	Current delivered by external power supply	0.5	—	—	A
T	Operating ambient temperature	–40	—	85	°C

4.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}	Low-level output voltage	—	—	0.1 × VDD[1]	V

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Table 6 – cont'd from previous page

Symbol	Parameter		Min	Typ	Max	Unit
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, output drive strength set to the maximum)	VDD3P3_CPU power domain [1, 2]	—	40	—	mA
		VDD3P3_RTC power domain [1, 2]	—	40	—	mA
		VDD_SDIO power domain [1, 3]	—	20	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, output drive strength set to the maximum)		—	28	—	mA
R_{PU}	Resistance of internal pull-up resistor		—	45	—	kΩ
R_{PD}	Resistance of internal pull-down resistor		—	45	—	kΩ
V_{IL_nRST}	Low-level input voltage of CHIP_PU to shut down the chip		—	—	0.6	V

[1] Please see Appendix IO MUX of *ESP32 Series Datasheet* for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.

[2] For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, V_{OH}>=2.64 V, as the number of current-source pins increases.

[3] Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

4.4 Current Consumption Characteristics

Owing to the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section *RTC and Low-Power Management* in *ESP32 Series Datasheet*.

Table 7: Current Consumption Depending on RF Modes

Work mode	Description		Average (mA)	Peak (mA)
Active (RF working)	TX	802.11b, 20 MHz, 1 Mbps, @19.5 dBm	233	368
		802.11g, 20 MHz, 54 Mbps, @14 dBm	181	258
		802.11n, 20 MHz, MCS7, @13 dBm	178	248
		802.11n, 40 MHz, MCS7, @13 dBm	162	205
	RX[2]	802.11b/g/n, 20 MHz	110	111
		802.11n, 40 MHz	116	117

[1] The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 50% duty cycle.

[2] The current consumption figures in RX mode are for cases when the peripherals are disabled and the CPU idle.

Table 8: Current Consumption Depending on Work Modes

Work mode	Description		Current consumption (Typ)
Modem-sleep [1, 2]	The CPU is powered on [3]	240 MHz	30 ~ 68 mA
		160 MHz	27 ~ 44 mA
		Normal speed: 80 MHz	20 ~ 31 mA
Light-sleep	—		0.8 mA
Deep-sleep	The ULP coprocessor is powered on [4]		150 μA
	ULP sensor-monitored pattern [5]		100 μA @1% duty
	RTC timer + RTC memory		10 μA
	RTC timer only		5 μA
Power off	CHIP_PU is set to low level, the chip is powered off		1 μA

[1] The current consumption figures in Modem-sleep mode are for cases where the CPU is powered on and the cache idle.

[2] When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, current consumption changes accordingly.

[3] In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.

[4] During Deep-sleep, when the ULP coprocessor is powered on, peripherals such as GPIO and RTC I2C are able to operate.

[5] The "ULP sensor-monitored pattern" refers to the mode where the ULP coprocessor or the sensor works periodically. When ADC works with a duty cycle of 1%, the typical current consumption is 100 μA.

4.5 Wi-Fi RF Characteristics

4.5.1 Wi-Fi RF Standards

Table 9: Wi-Fi RF Standards

Name		Description
Center frequency range of operating channel *		2412 ~ 2484 MHz
Wi-Fi wireless standard		IEEE 802.11b/g/n
Data rate	20 MHz	11b: 1, 2, 5.5, 11 Mbps 11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps 11n: MCS0-7, 72.2 Mbps (Max)
	40 MHz	11n: MCS0-7, 150 Mbps (Max)
Antenna type		PCB antenna

* Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software.

4.5.2 Transmitter Characteristics

Target TX power is configurable based on device or certification requirements. The default characteristics are provided in Table 10.

Table 10: TX Power Characteristics

Rate	Typ (dBm)
11b, 1 Mbps	19.5
11b, 11 Mbps	19.5
11g, 6 Mbps	18
11g, 54 Mbps	14
11n, HT20, MCS0	18
11n, HT20, MCS7	13
11n, HT40, MCS0	18
11n, HT40, MCS7	13

4.5.3 Receiver Characteristics

Table 11: RX Sensitivity Characteristics

Rate	Typ (dBm)
1 Mbps	–97
2 Mbps	–94
5.5 Mbps	–91
11 Mbps	–88
6 Mbps	–92
9 Mbps	–91
12 Mbps	–89
18 Mbps	–87
24 Mbps	–84
36 Mbps	–80
48 Mbps	–76
54 Mbps	–75
11n, HT20, MCS0	–91
11n, HT20, MCS1	–88
11n, HT20, MCS2	–85
11n, HT20, MCS3	–83
11n, HT20, MCS4	–80
11n, HT20, MCS5	–75
11n, HT20, MCS6	–74
11n, HT20, MCS7	–72
11n, HT40, MCS0	–88
11n, HT40, MCS1	–85
11n, HT40, MCS2	–82
11n, HT40, MCS3	–80
11n, HT40, MCS4	–76
11n, HT40, MCS5	–72
11n, HT40, MCS6	–71

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Table 11 – cont'd from previous page

Rate	Typ (dBm)
11n, HT40, MCS7	–69

Table 12: RX Maximum Input Level

Rate	Typ (dBm)
11b, 1 Mbps	5
11b, 11 Mbps	5
11g, 6 Mbps	0
11g, 54 Mbps	–8
11n, HT20, MCS0	0
11n, HT20, MCS7	–8
11n, HT40, MCS0	0
11n, HT40, MCS7	–8

Table 13: Adjacent Channel Rejection

Rate	Typ (dB)
11b, 11 Mbps	35
11g, 6 Mbps	27
11g, 54 Mbps	13
11n, HT20, MCS0	27
11n, HT20, MCS7	12
11n, HT40, MCS0	16
11n, HT40, MCS7	7

4.6 Bluetooth Radio

4.6.1 Receiver – Basic Data Rate

Table 14: Receiver Characteristics – Basic Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @0.1% BER	—	–90	–89	–88	dBm
Maximum received signal @0.1% BER	—	0	—	—	dBm
Co-channel C/I	—	—	+7	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	—	–6	dB
	F = F0 – 1 MHz	—	—	–6	dB
	F = F0 + 2 MHz	—	—	–25	dB
	F = F0 – 2 MHz	—	—	–33	dB
	F = F0 + 3 MHz	—	—	–25	dB
	F = F0 – 3 MHz	—	—	–45	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	—	—	dBm

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Table 14 – cont'd from previous page

Parameter	Conditions	Min	Typ	Max	Unit
	2000 MHz ~ 2400 MHz	–27	—	—	dBm
	2500 MHz ~ 3000 MHz	–27	—	—	dBm
	3000 MHz ~ 12.5 GHz	–10	—	—	dBm
Intermodulation	—	–36	—	—	dBm

4.6.2 Transmitter – Basic Data Rate

Table 15: Transmitter Characteristics – Basic Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power*	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
+20 dB bandwidth	—	—	0.9	—	MHz
Adjacent channel transmit power	F = F0 ± 2 MHz	—	–55	—	dBm
	F = F0 ± 3 MHz	—	–55	—	dBm
	F = F0 ± > 3 MHz	—	–59	—	dBm
$\Delta f1_{avg}$	—	—	—	155	kHz
$\Delta f2_{max}$	—	127	—	—	kHz
$\Delta f2_{avg}/\Delta f1_{avg}$	—	—	0.92	—	—
ICFT	—	—	–7	—	kHz
Drift rate	—	—	0.7	—	kHz/50 μs
Drift (DH1)	—	—	6	—	kHz
Drift (DH5)	—	—	6	—	kHz

* There are a total of eight power levels from 0 to 7, and the transmit power ranges from –12 dBm to 9 dBm. When the power level rises by 1, the transmit power increases by 3 dB. Power level 4 is used by default and the corresponding transmit power is 0 dBm.

4.6.3 Receiver – Enhanced Data Rate

Table 16: Receiver Characteristics – Enhanced Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
π/4 DQPSK					
Sensitivity @0.01% BER	—	–90	–89	–88	dBm
Maximum received signal @0.01% BER	—	—	0	—	dBm
Co-channel C/I	—	—	11	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–7	—	dB
	F = F0 – 1 MHz	—	–7	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–35	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–45	—	dB

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Table 16 – cont'd from previous page

Parameter	Conditions	Min	Typ	Max	Unit
8DPSK					
Sensitivity @0.01% BER	—	–84	–83	–82	dBm
Maximum received signal @0.01% BER	—	—	–5	—	dBm
C/I c-channel	—	—	18	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	2	—	dB
	F = F0 – 1 MHz	—	2	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–25	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–38	—	dB

4.6.4 Transmitter – Enhanced Data Rate

Table 17: Transmitter Characteristics – Enhanced Data Rate

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power (see note under Table 15)	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
π/4 DQPSK max w0	—	—	–0.72	—	kHz
π/4 DQPSK max wi	—	—	–6	—	kHz
π/4 DQPSK max |wi + w0|	—	—	–7.42	—	kHz
8DPSK max w0	—	—	0.7	—	kHz
8DPSK max wi	—	—	–9.6	—	kHz
8DPSK max |wi + w0|	—	—	–10	—	kHz
π/4 DQPSK modulation accuracy	RMS DEVM	—	4.28	—	%
	99% DEVM	—	100	—	%
	Peak DEVM	—	13.3	—	%
8 DPSK modulation accuracy	RMS DEVM	—	5.8	—	%
	99% DEVM	—	100	—	%
	Peak DEVM	—	14	—	%
In-band spurious emissions	F = F0 ± 1 MHz	—	–46	—	dBm
	F = F0 ± 2 MHz	—	–44	—	dBm
	F = F0 ± 3 MHz	—	–49	—	dBm
	F = F0 +/– > 3 MHz	—	—	–53	dBm
EDR differential phase coding	—	—	100	—	%

4.7 Bluetooth LE Radio

4.7.1 Receiver

Table 18: Receiver Characteristics – Bluetooth LE

Parameter	Conditions	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	–94	–93	–92	dBm
Maximum received signal @30.8% PER	—	0	—	—	dBm
Co-channel C/I	—	—	+10	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–5	—	dB
	F = F0 – 1 MHz	—	–5	—	dB
	F = F0 + 2 MHz	—	–25	—	dB
	F = F0 – 2 MHz	—	–35	—	dB
	F = F0 + 3 MHz	—	–25	—	dB
	F = F0 – 3 MHz	—	–45	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	–10	—	—	dBm
	2000 MHz ~ 2400 MHz	–27	—	—	dBm
	2500 MHz ~ 3000 MHz	–27	—	—	dBm
	3000 MHz ~ 12.5 GHz	–10	—	—	dBm
Intermodulation	—	–36	—	—	dBm

4.7.2 Transmitter

Table 19: Transmitter Characteristics – Bluetooth LE

Parameter	Conditions	Min	Typ	Max	Unit
RF transmit power (see note under Table 15)	—	—	0	—	dBm
Gain control step	—	—	3	—	dB
RF power control range	—	–12	—	+9	dBm
Adjacent channel transmit power	F = F0 ± 2 MHz	—	–55	—	dBm
	F = F0 ± 3 MHz	—	–57	—	dBm
	F = F0 ± > 3 MHz	—	–59	—	dBm
$\Delta\ f1_{avg}$	—	—	—	265	kHz
$\Delta\ f2_{max}$	—	210	—	—	kHz
$\Delta\ f2_{avg}/\Delta\ f1_{avg}$	—	—	+0.92	—	—
ICFT	—	—	–10	—	kHz
Drift rate	—	—	0.7	—	kHz/50 μs
Drift	—	—	2	—	kHz

5 Peripheral Schematics

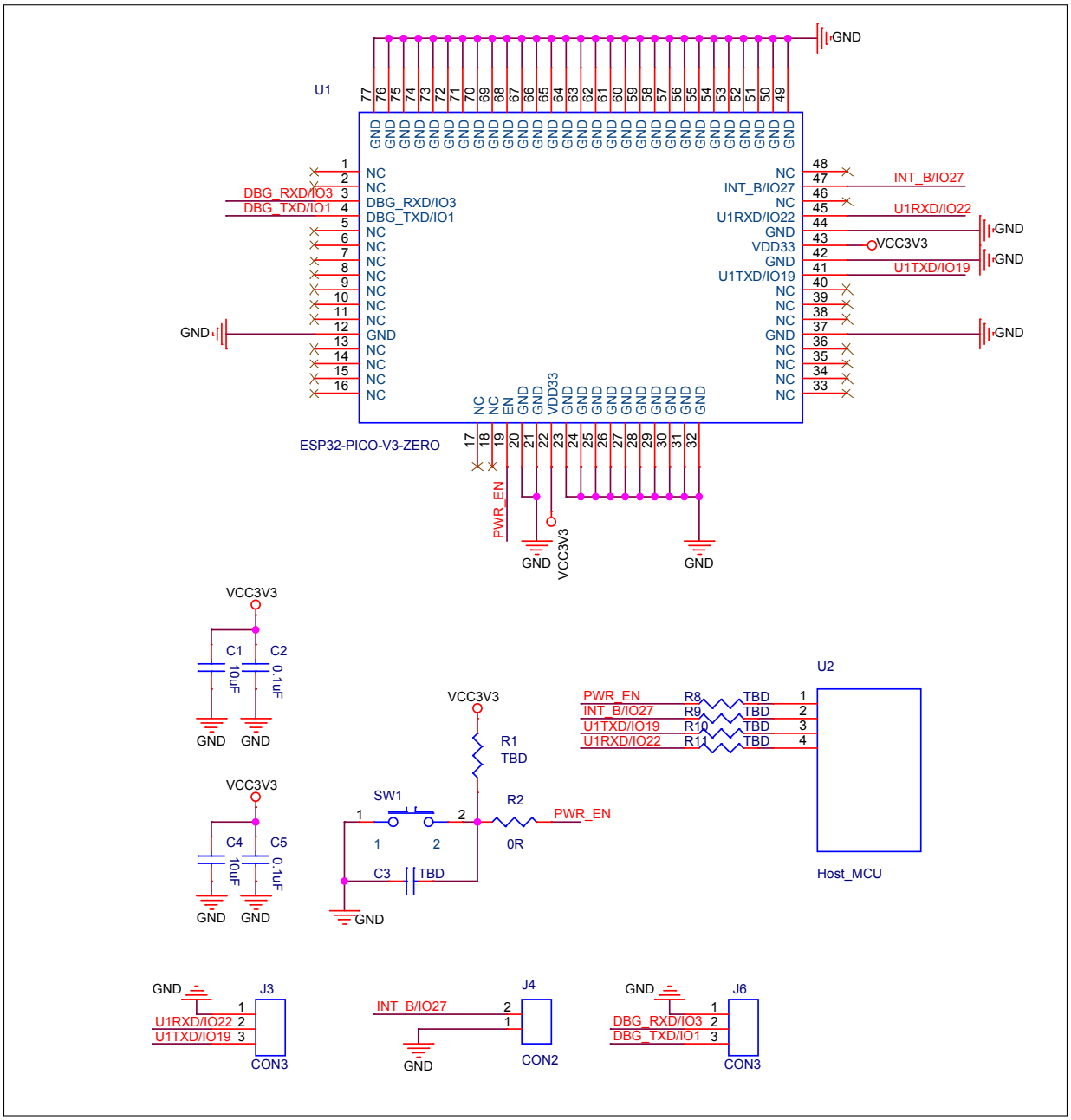

Figure 4: Peripheral Schematics

- Soldering EPAD Pin 73 to the ground of the base board is not a must. If you choose to solder it, please apply the correct amount of soldering paste. Too much soldering paste may increase the gap between the module and the baseboard. As a result, the adhesion between other pins and the baseboard may be poor.
- To ensure that the power supply to the ESP32 chip is stable during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32 Series Datasheet*.

6 Physical Dimensions and PCB Land Pattern

6.1 Physical Dimensions

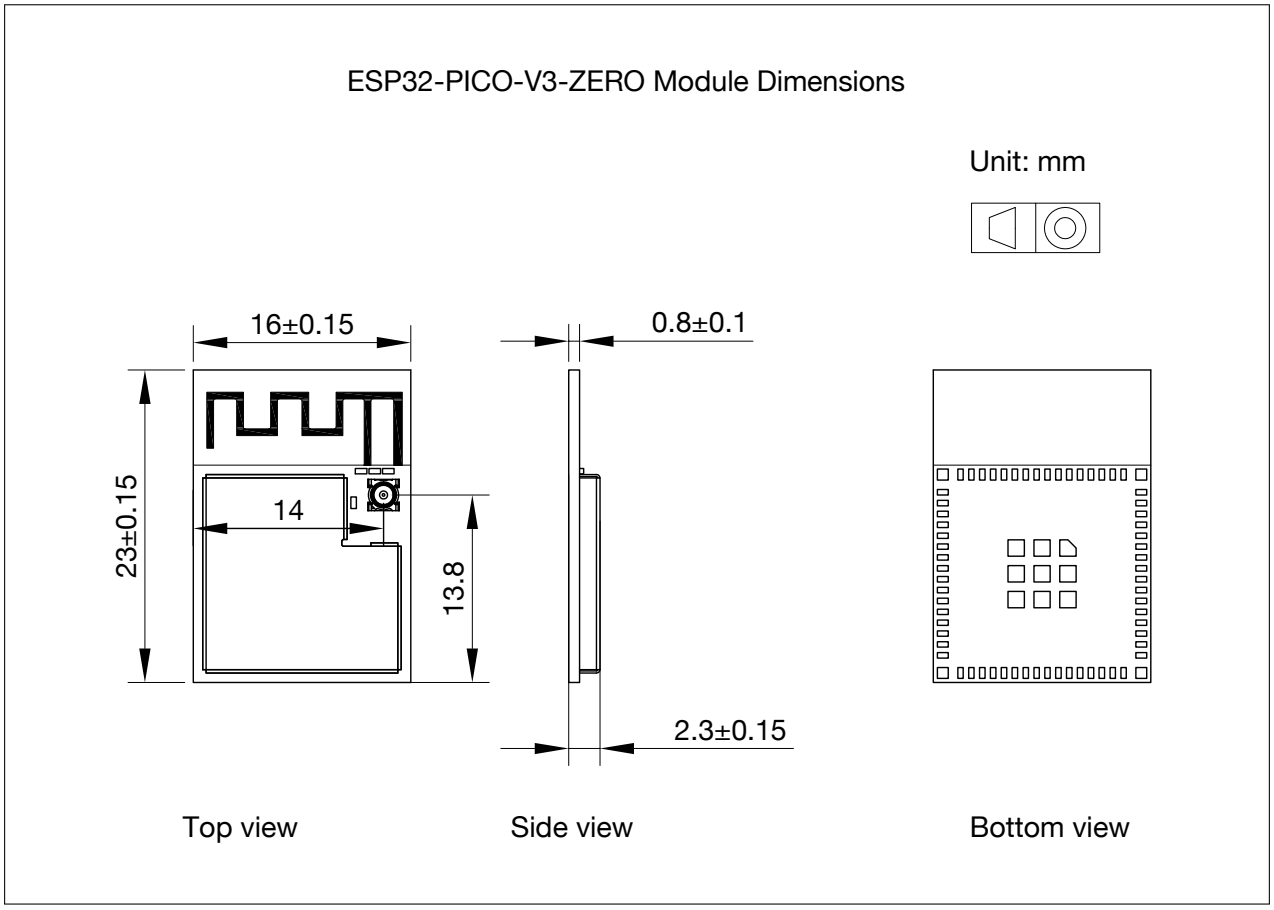

Figure 5: Physical Dimensions

Note:
For information about tape, reel, and product marking, please refer to *Espressif Module Package Information*.

6.2 PCB Layout

6.2.1 Recommended PCB Land Pattern

This section provides the following resources for your reference:

- Figures for recommended PCB land patterns with all the dimensions needed for PCB design. See Figure 6 *Recommended PCB Land Pattern*.
- Source files of recommended PCB land patterns to measure dimensions not covered in Figure 6. You can view the source files for ESP32-PICO-V3-ZERO with Autodesk Viewer.
- 3D models of ESP32-PICO-V3-ZERO. Please make sure that you download the 3D model file in .STEP format (beware that some browsers might add .txt).

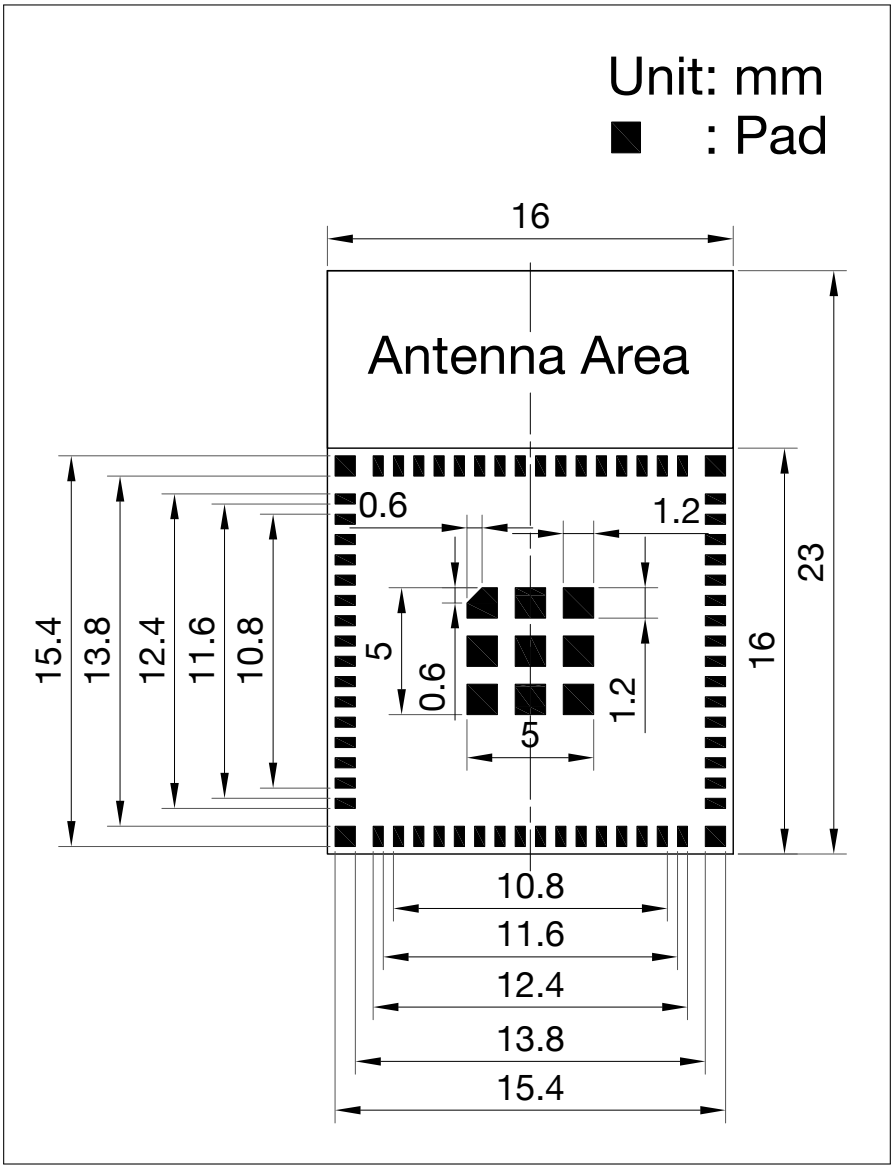

Figure 6: Recommended PCB Land Pattern

6.2.2 PCB Layout Guide

To achieve the optimum RF performance on a device with on-board antenna, please follow the guidelines below.

The module uses an inverted-F antenna design, and the antenna area of the module should have specific placement against the base board. The feed point of the antenna should be as close to the board as possible. The PCB antenna area should be placed outside the base board whenever possible while the module be put as close as possible to the edge of the base board.

As is shown in Figure 7, examples 3 and 4 of the module position on the base board are highly recommended, while examples 1, 2, and 5 are not recommended.

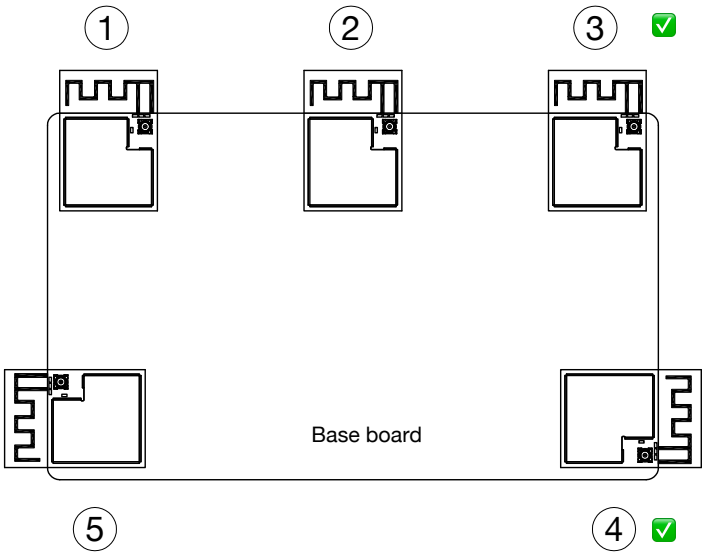

Figure 7: Module Placement on a Base Board

If the positions recommended above are not possible, then please make sure that the module is not covered by any metal shell and that a clearance area (without copper, routing, or components) outside the antenna is large enough, as shown in Figure 8. In addition, if there is base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna.

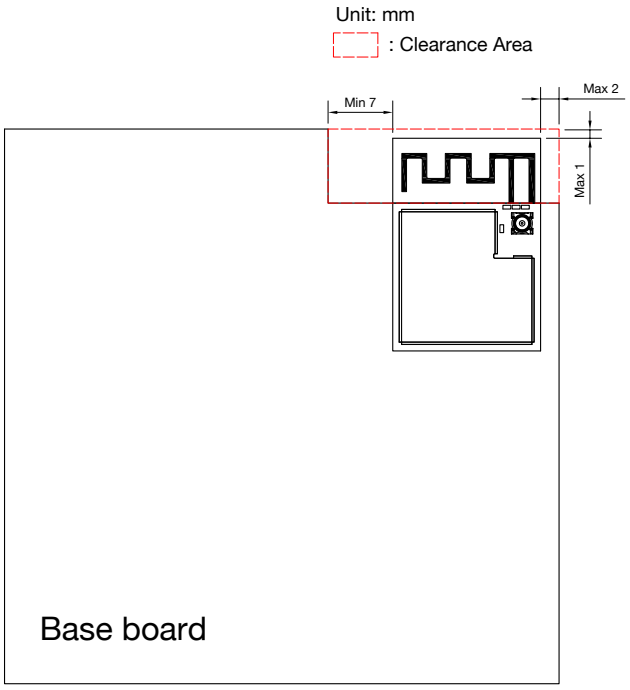

Figure 8: Keepout Zone for Module's Antenna on the Base Board

If the PCB layout does not follow the above rules, then RF throughput and RF range testing should be performed to ensure that the end product performance is satisfactory. When designing an end product, pay attention to the impact of enclosure on the antenna and verify the device performance by making RF verification.

6.3 Dimensions of RF Test Connector

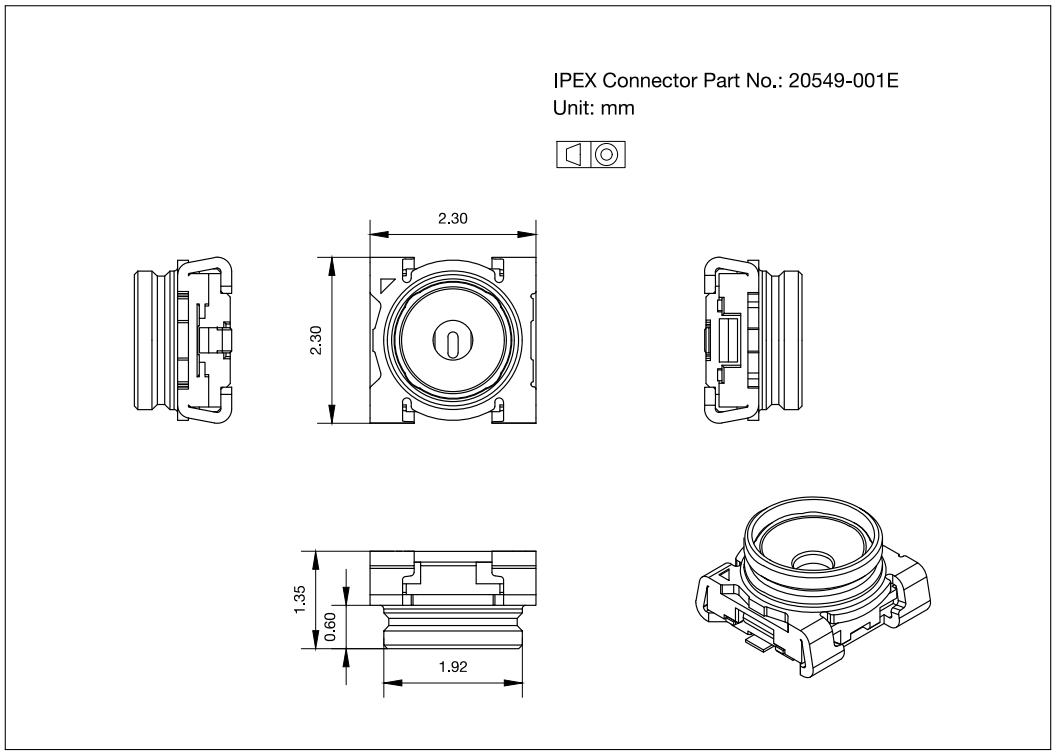

Figure 9: Dimensions of RF Test Connector

7 Product Handling

7.1 Storage Conditions

The products sealed in moisture barrier bags (MBB) should be stored in a non-condensing atmospheric environment of < 40 °C and 90%RH. The module is rated at the moisture sensitivity level (MSL) of 3.

After unpacking, the module must be soldered within 168 hours with the factory conditions 25 ± 5 °C and 60 %RH. If the above conditions are not met, the module needs to be baked.

7.2 Electrostatic Discharge (ESD)

- Human body model (HBM): ±2000 V
- Charged-device model (CDM): ±500 V

7.3 Reflow Profile

Solder the module in a single reflow.

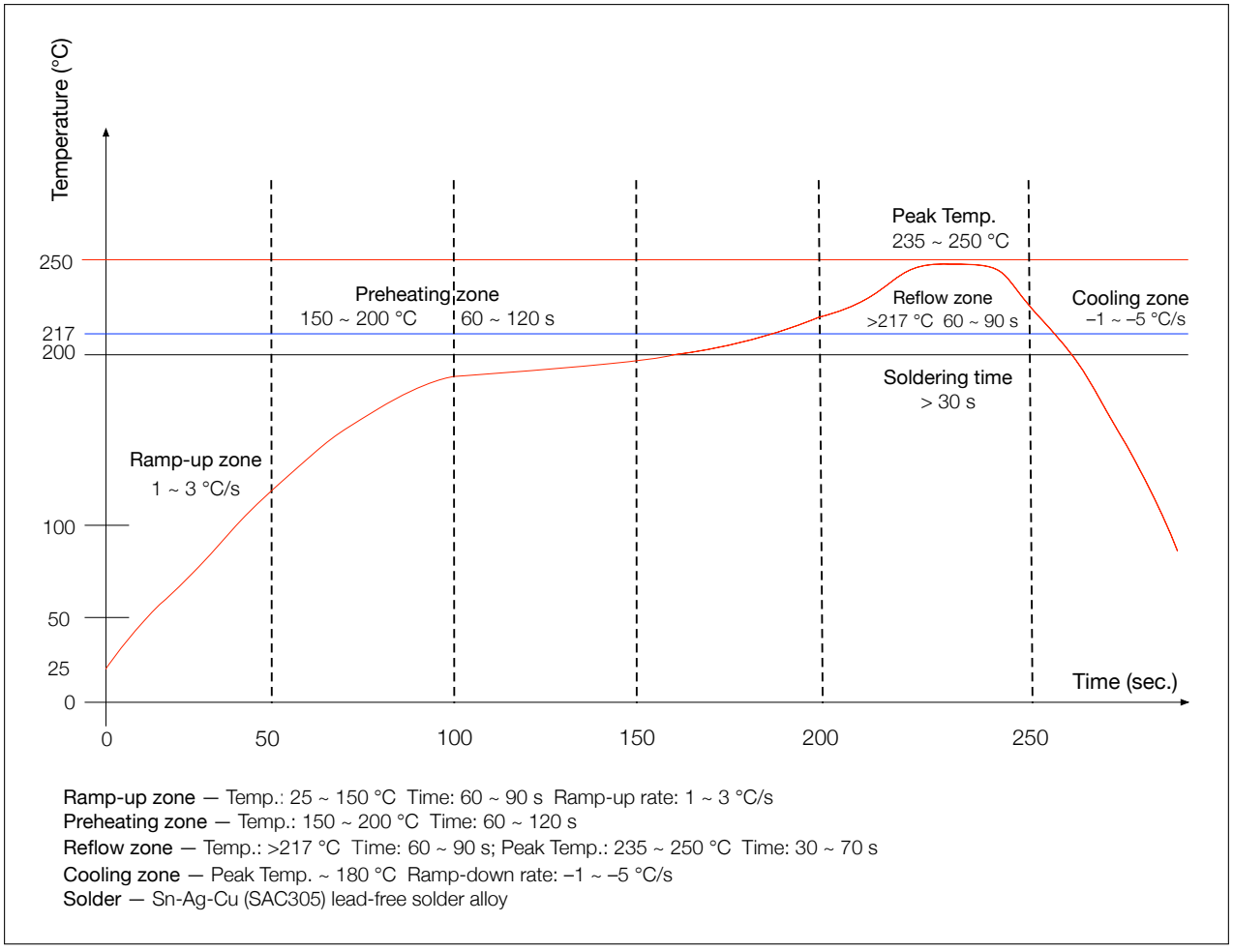

Figure 10: Reflow Profile

7.4 Ultrasonic Vibration

Avoid exposing Espressif modules to vibration from ultrasonic equipment, such as ultrasonic welders or ultrasonic cleaners. This vibration may induce resonance in the in-module crystal and lead to its malfunction or even failure. As a consequence, **the module may stop working or its performance may deteriorate**.

8 Related Documentation and Resources

Related Documentation

- ESP32 Series Datasheet – Specifications of the ESP32 hardware.
- ESP32 Technical Reference Manual – Detailed information on how to use the ESP32 memory and peripherals.
- ESP32 Hardware Design Guidelines – Guidelines on how to integrate the ESP32 into your hardware product.
- ESP32 ECO and Workarounds for Bugs – Correction of ESP32 design errors.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns
- *ESP32 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32 Series SoCs* – Browse through all ESP32 SoCs.
  https://espressif.com/en/products/socs?id=ESP32
- *ESP32 Series Modules* – Browse through all ESP32-based modules.
  https://espressif.com/en/products/modules?id=ESP32
- *ESP32 Series DevKits* – Browse through all ESP32-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release notes
2023-08-29	v1.4	• Added Section 3.3 *Strapping Pins* • Section 5 *Peripheral Schematics*: Added a note about EPAD soldering • Section 6.2.1 *Recommended PCB Land Pattern*: Added source files of PCB land patterns and 3D models of the module • Added Section 7.4 *Ultrasonic Vibration*
2022-02-22	v1.3	Added a note regarding the RF test connector in Section 1.1 Updated Figure 1, Table 6, and Table 9
2021-11-08	v1.2	Added a note below Figure 5: *Physical Dimensions* Updated Table 5: *Recommended Operating Conditions* Upgraded document formatting
2021-02-09	v1.1	Deleted Reset Circuit and Discharge Circuit for VDD33 Rail in Section 5 *Peripheral Schematics* Modified the note below Figure 10 *Reflow Profile*
2020-11-03	v1.0	First release

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