ESP-PSRAM16H

Datasheet

Version 1.1
Espressif Systems

About This Document

This document introduces the specifications of ESP-PSRAM16H.

Release Notes

Date	Version	Release notes
2020-04-15	V1.0	First release
2020-10-13	V1.1	Updated Appendix–Device Marking Convention

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Table of Contents

1. Introduction

ESP-PSRAM16H is a 16 Mbit serial pseudo SRAM device that is fabricated using very high-performance, high-reliability CMOS technology. ESP-PSRAM16H operates at 3.3 V and can support up to 133 MHz clock rate.

ESP-PSRAM16H is accessible via a simple Serial Peripheral Interface (SPI) compatible serial bus. Additionally, Quad Peripheral Interface (QPI) is supported if the application needs faster data rates. The device also supports unlimited reads and writes to the memory array.

Table 1-1. Ordering Information of ESP-PSRAM16H

Part number	Product density	Package type	Maximum Clock rate	Operating temperature	Product carrier	Green code	Operating voltage	Read/Write operation mode	SPI mode
ESP-PSRAM16H	16 Mbit	SOP8-150 mil	133 MHz	–40 ~ 85 °C	Tape & Reel	RoHS Compliant Package and Green/ Reach Package	3.3 V	512-byte Pages	Standard/ Quad SPI

2. Pin Description

Figure 2-1 shows the pin layout of ESP-PSRAM16H.

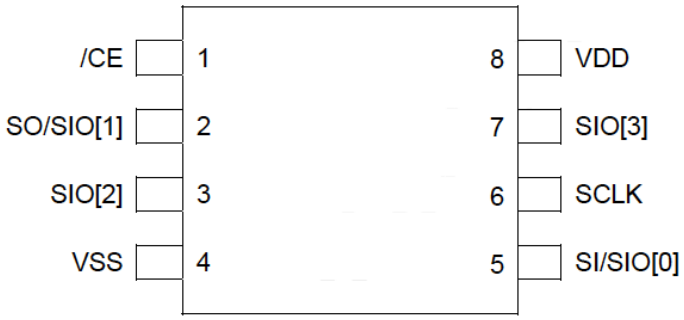


Figure 2-1. Pin Layout

Table 2-1. Signals Table

Pin	Signal Type	SPI Mode Function	QPI Mode Function
V_{DD}	Power	Power supply, 3.3 V.	
Vss	Ground	Core supply ground	
CE#	Input	Chip select signal, active low. When CE#=1, the chip is in standby state.	
CLK	Input	Clock signal	
SI/SIO[0]	I/O	Serial input	I/O[0]
SO/SIO[1]	I/O	Serial output	I/O[1]
SIO[2]	I/O	-	I/O[2]
SIO[3]	I/O	-	I/O[3]

3. Power-up Initialization

SPI/QPI products include an on-chip voltage sensor used to start the self-initialization process. When V_{DD} reaches a stable level at or above minimum V_{DD}, the device will require 150 µs and user-issued RESET operation to complete its self-initialization process. From the beginning of power ramp to the end of the 150-µs period, CLK should remain LOW, CE# should remain HIGH (track VDD within 200 mV) and SI/SO/SIO[3:0] should remain LOW.

After the 150-µs period the device is ready for normal operation.

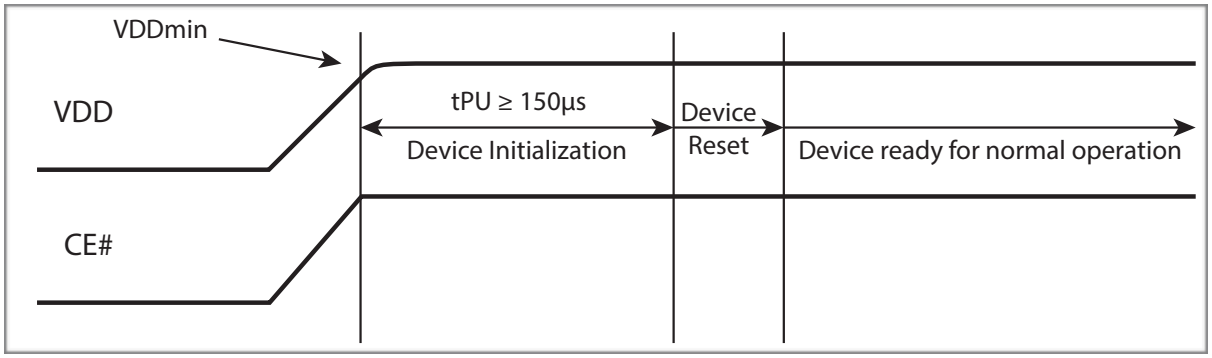


Figure 3-1. Power-up Initialization Timing

4. Interface Description

4.1. Address Space

SPI/QPI PSRAM device is byte-addressable. 16 MB device is addressed with A[20:0].

4.2. Page Size

The page size is 512 bytes. The device reads/writes in a wrap manner by default.

4.3. Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

4.4. Command/Address Latching Truth Table

The device recognizes the following commands specified by the various input methods.

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Addr	Wait Cycle	DIO	MAX Freq.	Cmd	Addr	Wait Cycle	DIO	MAX Freq.
Read	'h03	S	S	0	S	33					N/A
Fast Read	'h0B	S	S	8	S	133	Q	Q	4	Q	66
Fast Read Quad	'hEB	S	Q	6	Q	133	Q	Q	6	Q	133
Write	'h02	S	S	0	S	133	Q	Q	0	Q	133
Quad Write	'h38	S	Q	0	Q	133					Same as 'h02
Wrapped Read	'h8B	S	S	8	S	133	Q	Q	6	Q	133
Wrapped Write	'h82	S	S	0	S	133	Q	Q	0	Q	133
Mode Register Read	'hB5	S	S	8	S	133	Q	Q	6	Q	133
Mode Register Write	'hB1	S	S	0	S	133	Q	Q	0	Q	133
Enter Quad Mode	'h35	S	-	-	-	133					N/A

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Addr	Wait Cycle	DIO	MAX Freq.	Cmd	Addr	Wait Cycle	DIO	MAX Freq.
Exit Quad Mode	'hF5					N/A	Q	-	-	-	133
Reset Enable	'h66	S	-	-	-	133	Q	-	-	-	133
Reset	'h99	S	-	-	-	133	Q	-	-	-	133
Burst Length Toggle	'hC0	S	-	-	-	133	Q	-	-	-	133
Read ID	'h9F	S	S	0	S	33					N/A

📖 **Notes:**

1. S=Serial I/O; Q=Quad I/O.
2. The maximum clock frequency is 133 MHz. When burst commands cross page boundaries, the maximum input clock frequency is 84 MHz.

4.5. Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active command and set the device into standby. Not doing so will block internal refresh operations and cause memory failure.

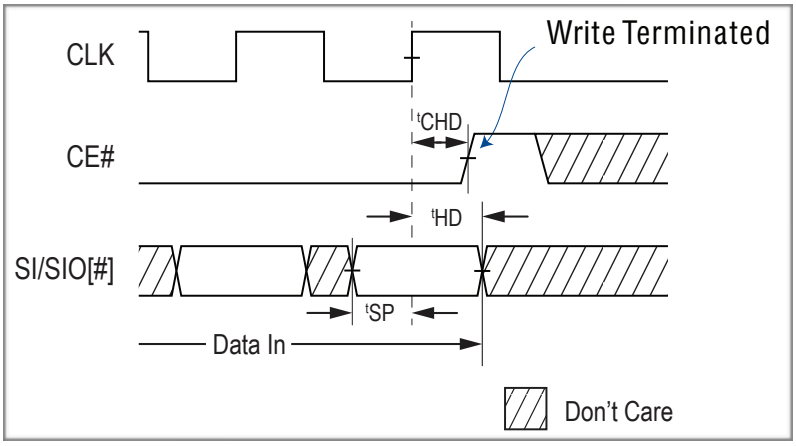


Figure 4-1. Write Command Termination

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a long CE# hold time($t_{CHD} > t_{ACLK} + t_{CLK}$)。

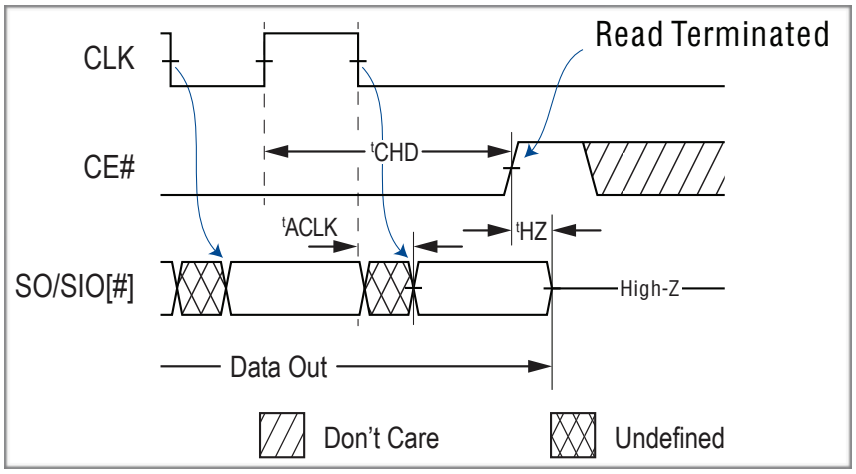


Figure 4-2. Read Command Termination

5. Mode Register Definition

Table 5-1. Mode Register Table

MR No.	MA[3:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	'h0	R/W	rsvd.	Wrap		rsvd.			DQ Zout	

Table 5-2. Wrap Burst Settings

MR0[6:5]	Wrapped length
00	16
01	32
10	64
11 (default)	512 (page size)

Table 5-3. DQ DQ Output Drive Strength

MR0[1:0]	Impedance
00 (default)	50 Ω
01	100 Ω
10	200 Ω
Others	reserved

6. Mode Register Operations

6.1. SPI MR Read Operation

For all reads, MR data will be available t_{ALCK} after the falling edge of CLK.

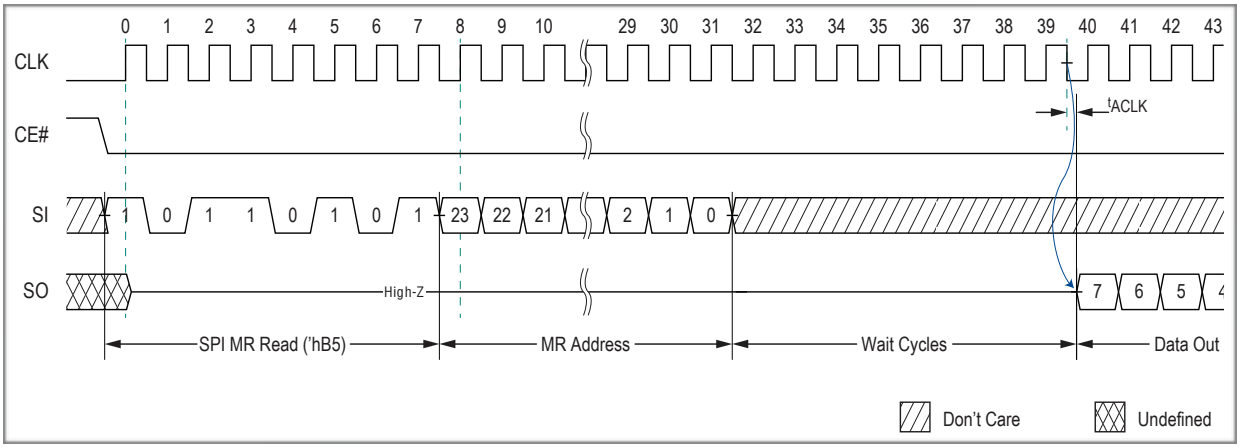


Figure 6-1. SPI MR Read 'hB5

6.2. SPI MR Write Operation

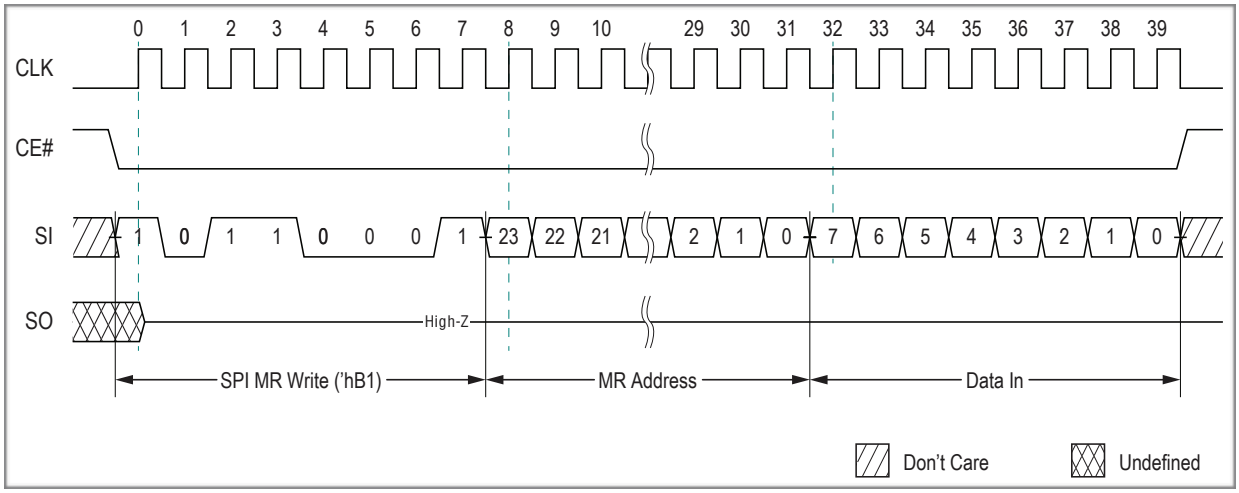


Figure 6-2. SPI MR Write 'hB1

6.3. QPI MR Read Operation

For all reads, MR data will be available t_{ALCK} after the falling edge of CLK.

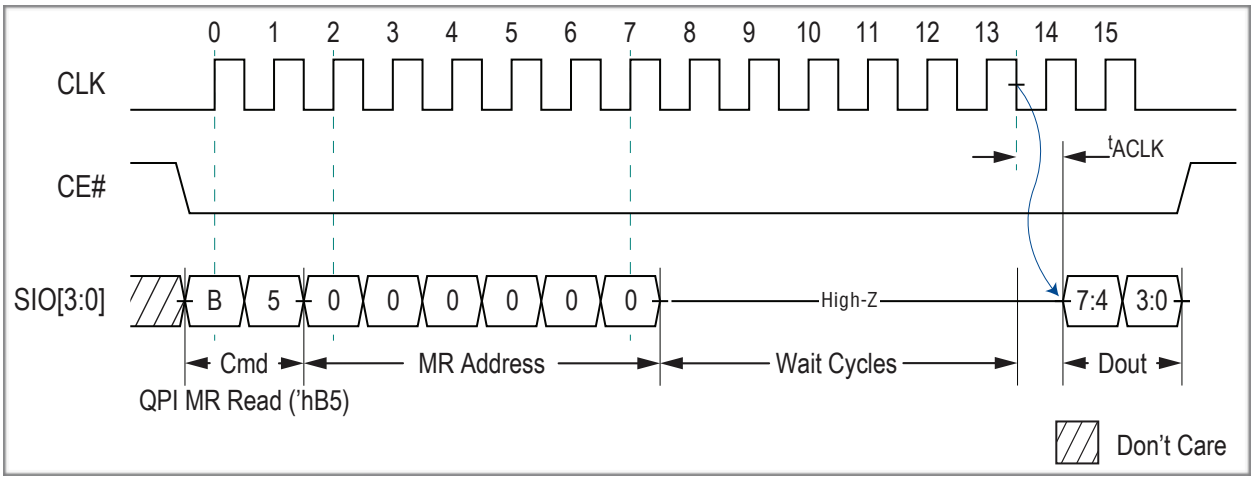


Figure 6-3. QPI MR Read 'hB5

6.4. QPI MR Write Operation

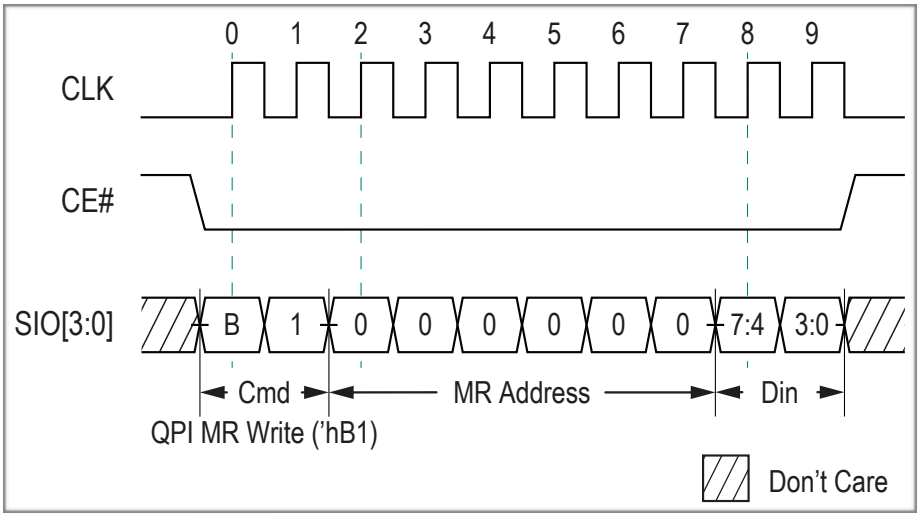


Figure 6-4. QPI MR Write 'hB1

7. SPI Mode Operations

The device powers up into SPI mode by default but can also be switched into QPI mode.

7.1. SPI Read Operations

For all reads, MR data will be available t_{ALCK} after the falling edge of CLK.

SPI Reads can be done in four ways:

- 'h03: Serial CMD, Serial Addr/IO, slow frequency
- 'h0B: Serial CMD, Serial Addr/IO, fast frequency
- 'hEB: Serial CMD, Quad Addr/IO, fast frequency
- 'h8B: Serial CMD, Serial Addr/IO, fast frequency

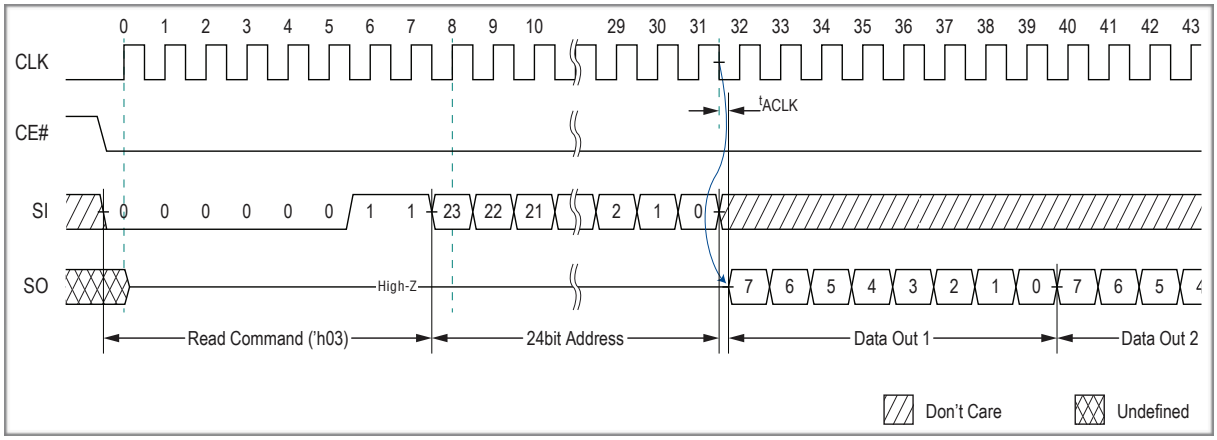


Figure 7-1. SPI Read 'h03 (max freq 33 MHz)

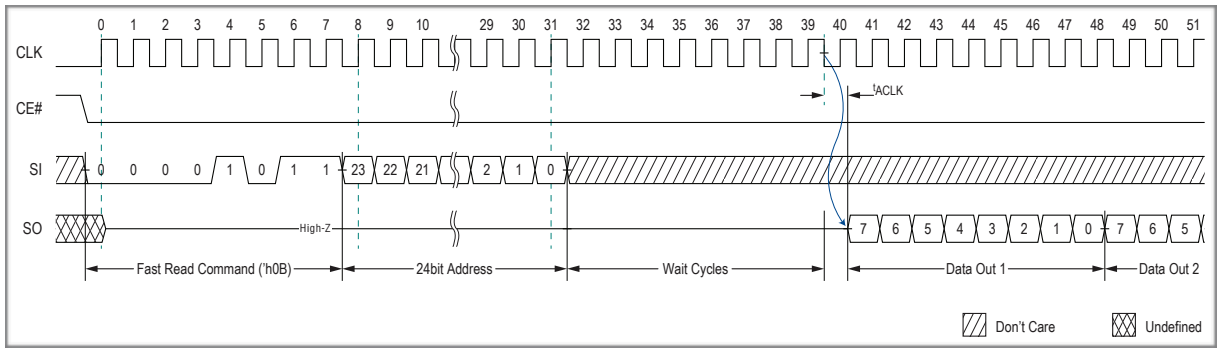


Figure 7-2. SPI Fast Read 'h0B (max freq 133 MHz)

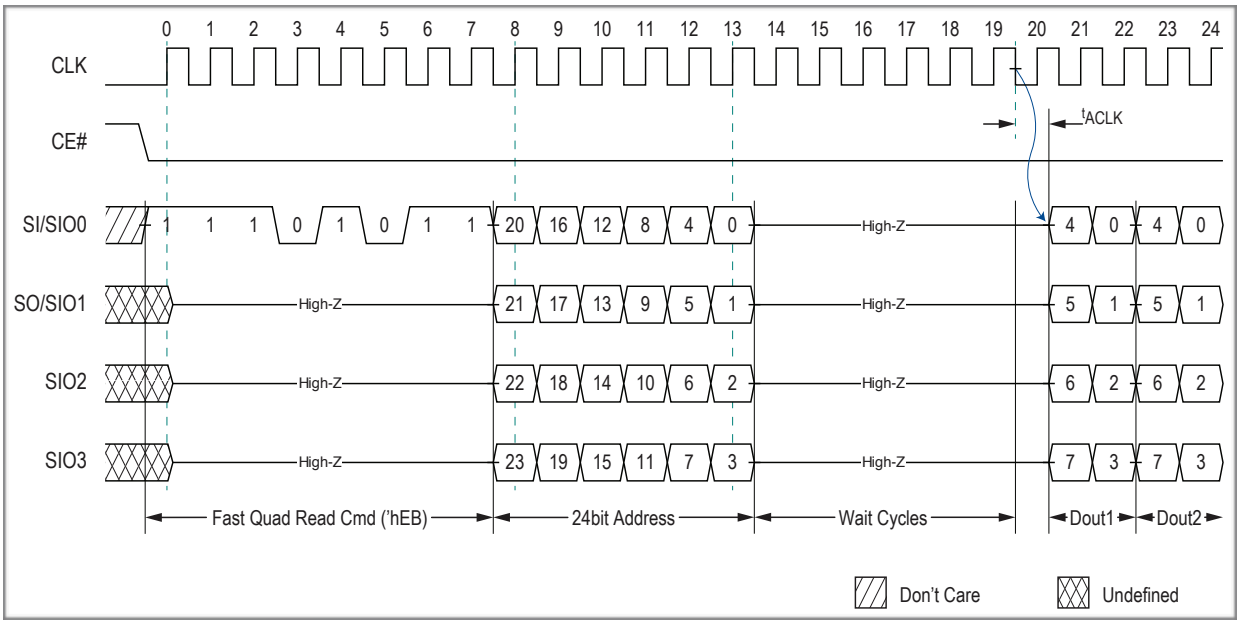


Figure 7-3. SPI Fast Quad Read 'hEB (max freq 133 MHz)

7.2. SPI Write Operations

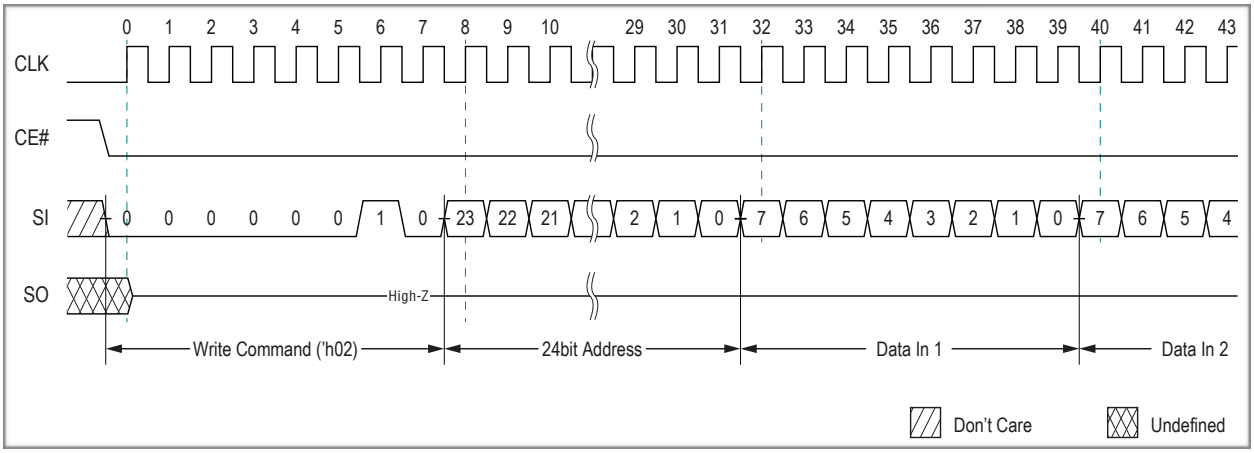


Figure 7-4. SPI Write 'h02

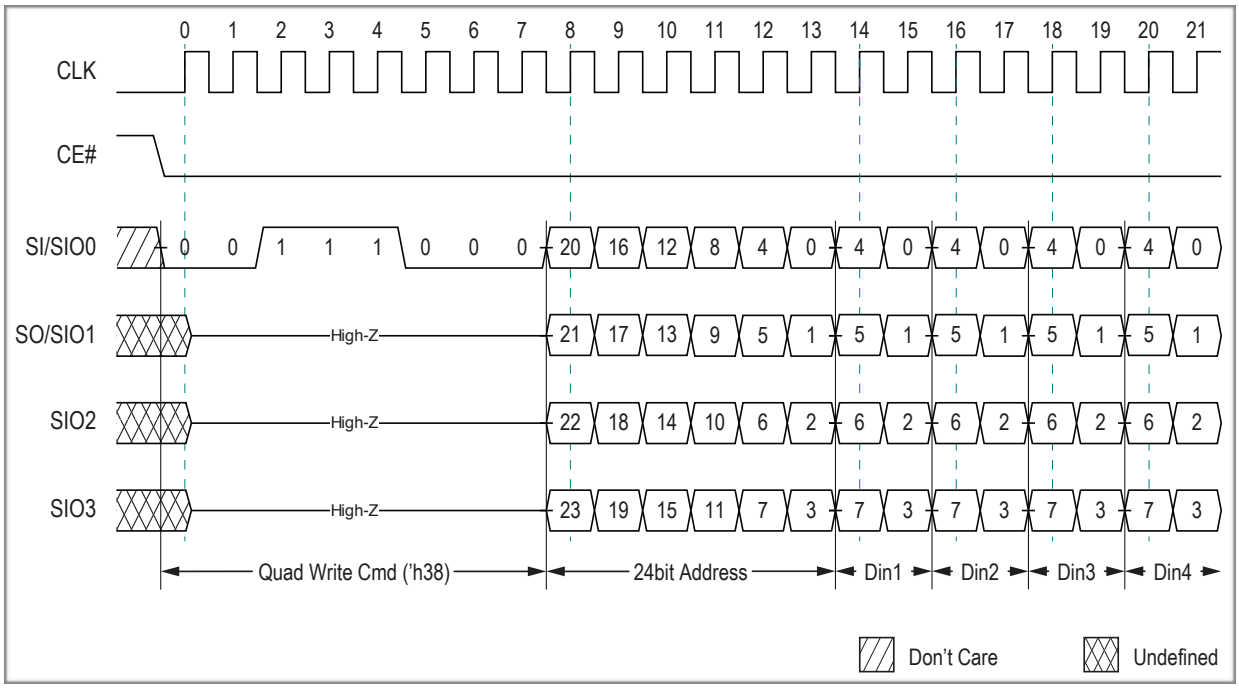


Figure 7-5. SPI Quad Write 'h38

7.3. SPI Quad Mode Enable Operation

This command switches the device into quad IO mode.

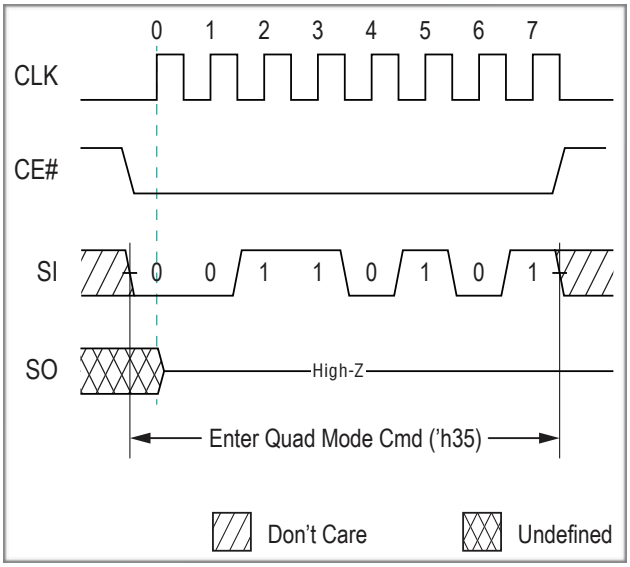


Figure 7-6. Quad Mode Enable 'h35 (available only in SPI mode)

8. QPI Mode Operations

8.1. QPI Read Operations

For all reads, MR data will be available t_{ALCK} after the falling edge of CLK.

QPI Reads can be done in four ways:

- 'h0B: Quad CMD, Quad IO, slow frequency
- 'hEB: Quad CMD, Addr & IO, fast frequency
- 'h8B: Quad CMD, Addr & IO, fast frequency

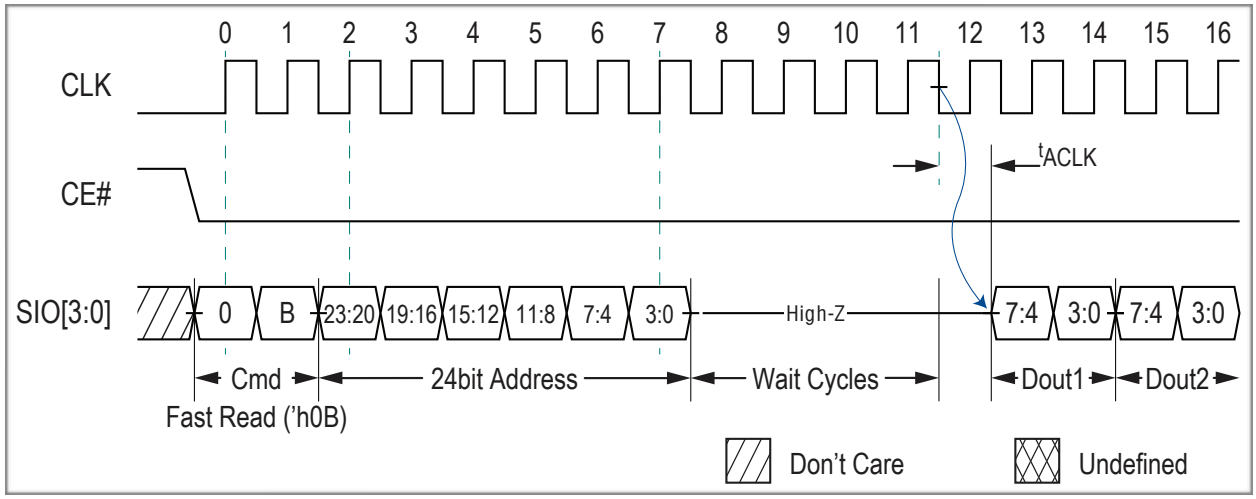


Figure 8-1. QPI Fast Read 'h0B (max freq 66 MHz)

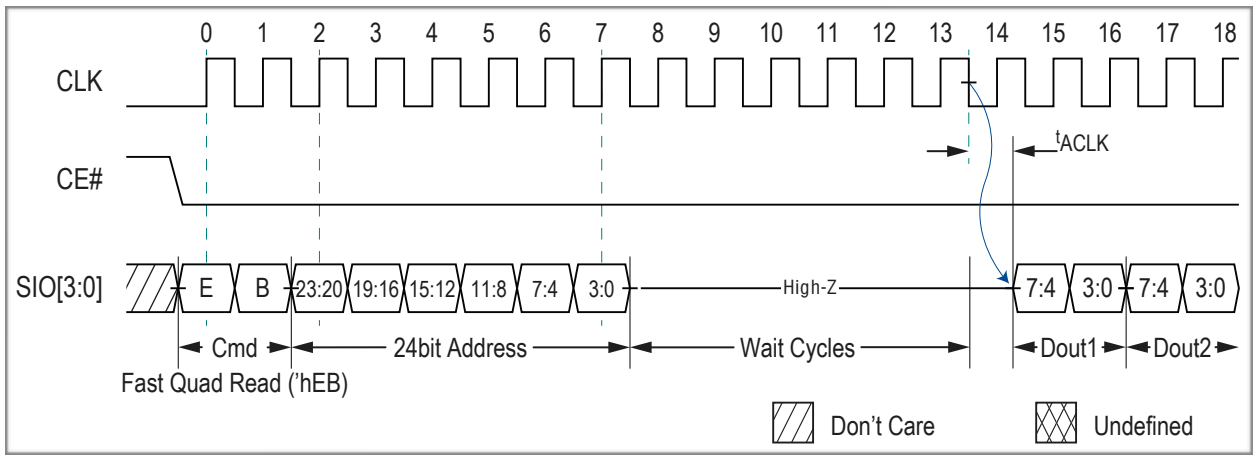


Figure 8-2. QPI Fast Quad Read 'hEB (max freq 133 MHz)

8.2. QPI Write Operations

QPI write command can be done in one of three ways:

- 'h02 or 'h38: Quad CMD, Addr & IO
- 'h82: Quad CMD, Addr & IO

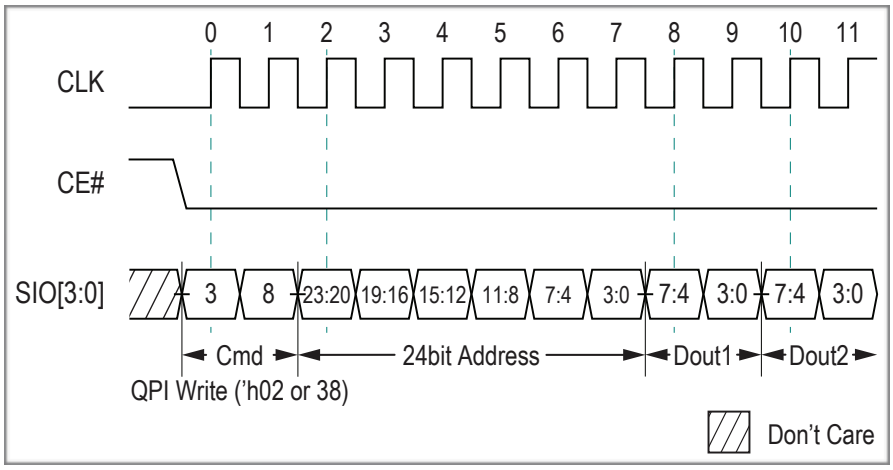


Figure 8-3. QPI Write

8.3. QPI Quad Mode Exit Operation

This command will switch the device back into serial IO mode.

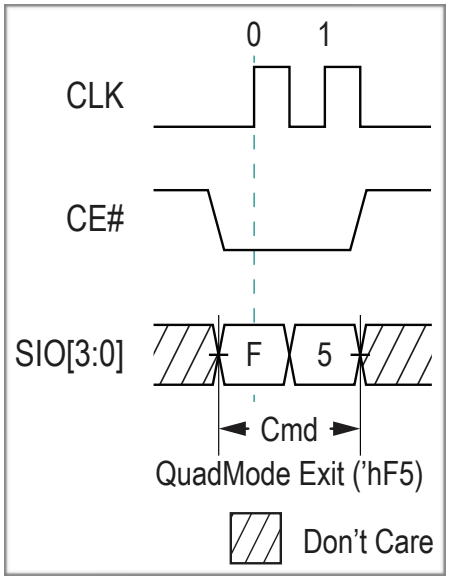


Figure 8-4. Quad Mode Exit 'hF5 (only available in QPI mode)

9. Reset Operation

The Reset operation is used as a system (software) reset that puts the device in SPI standby mode which is also the default mode after power-up. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

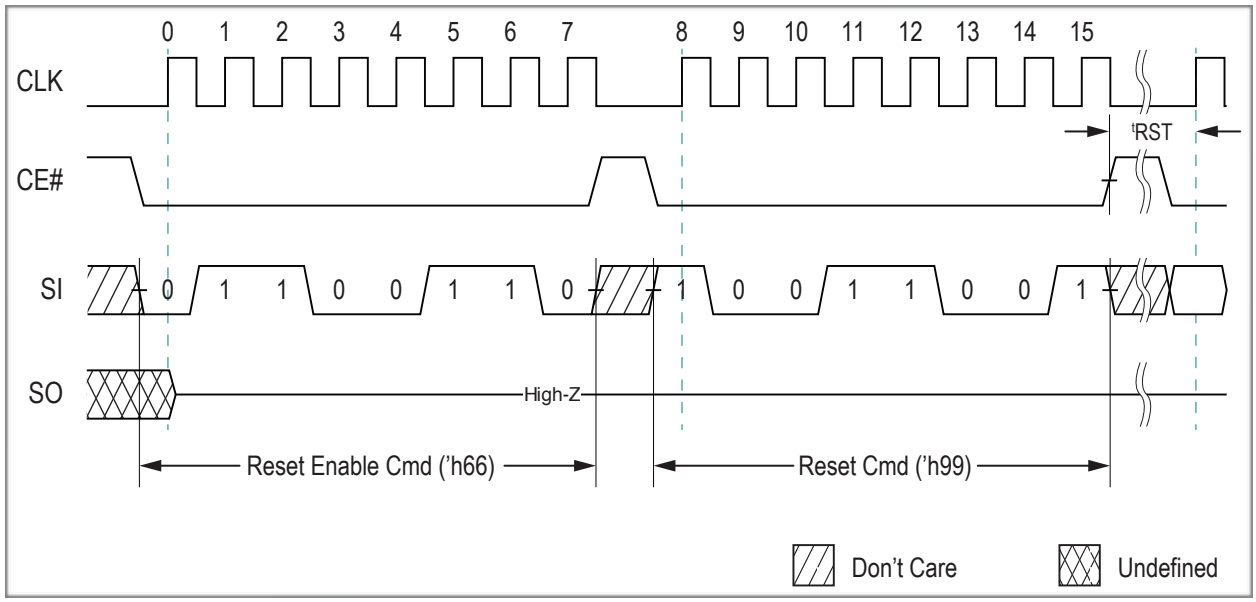


Figure 9-1. SPI Reset

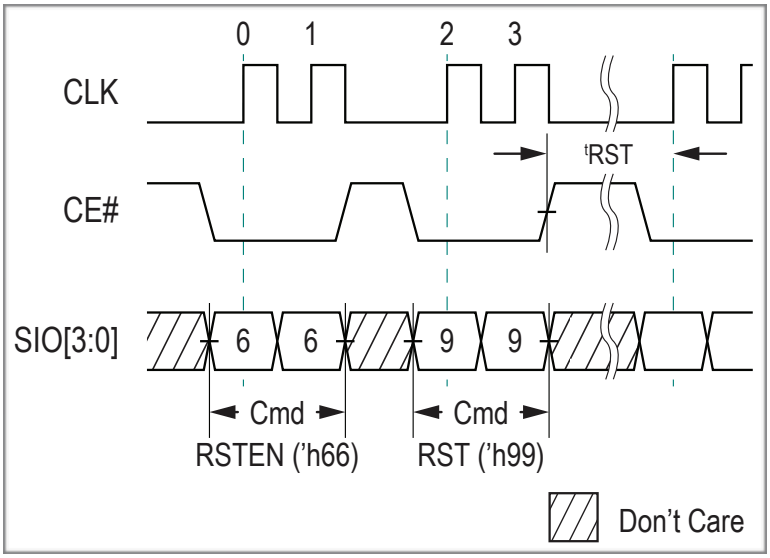


Figure 9-2. QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

10. Toggle Burst Length Operation

The Toggle Burst Length Operation switches the device's wrapped burst boundary between the Mode Register setting (default of 512 bytes CA[8:0]) and 32 (CA[4:0]) bytes or whatever is set in MR0[6:5] and a fixed value of 32 bytes.

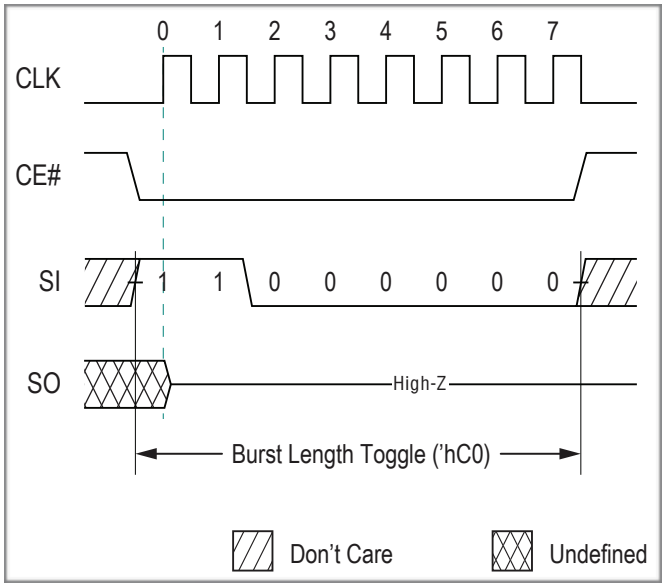


Figure 10-1. SPI Burst Length Toggle 'hC0

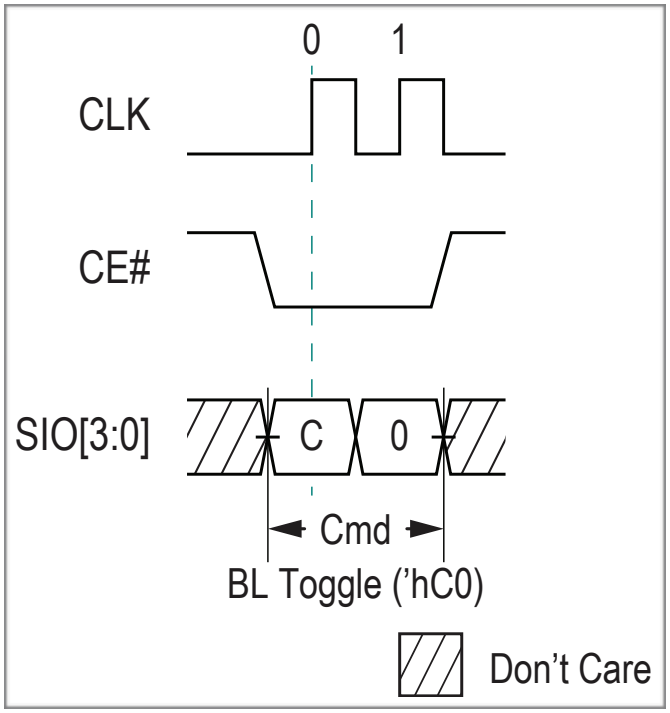


Figure 10-2. QPI Burst Length Toggle 'hC0

11. Read ID Operations

11.1. SPI Read ID Operation

This command is similar to Fast Read, but without the wait cycles and the device outputs EID value instead of data.

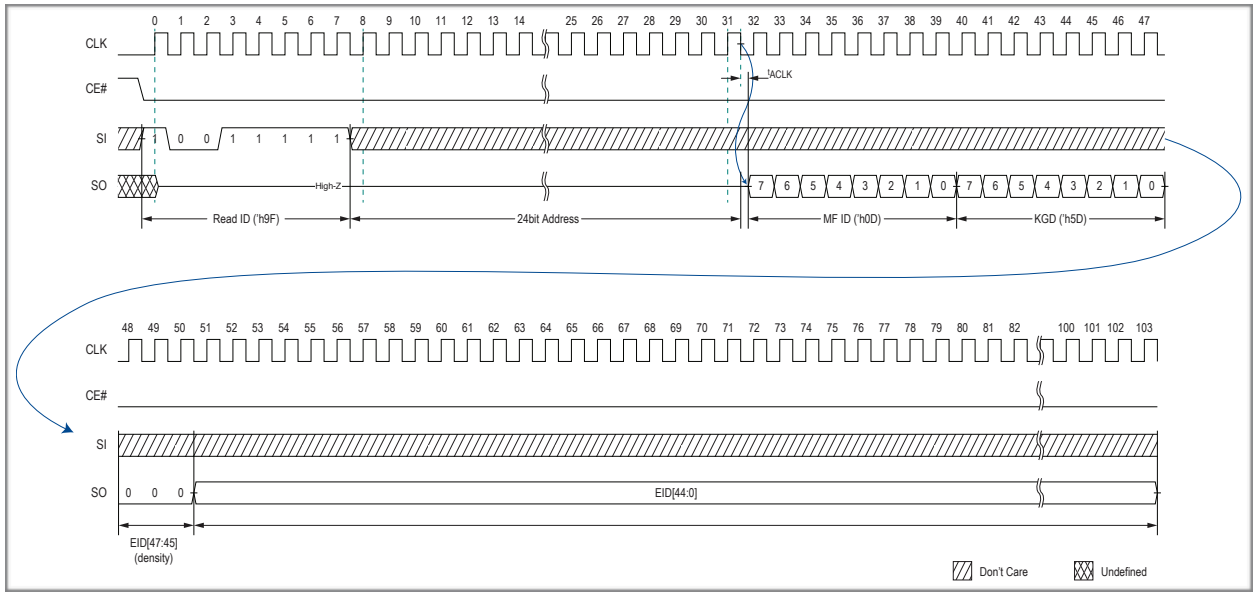


Figure 11-1. SPI Read ID 'h9F (available only in SPI mode)

11.2. QPI Read ID Operation

In the QPI mode, the QPI Read ID operation is the same as the QPI MR Read operation. Note about Dout [7]. MRR data output bit [7] outputs serial ID data every two clocks.

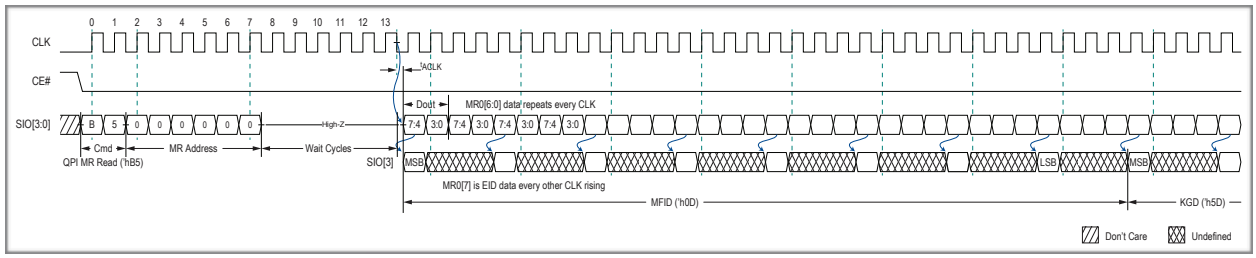


Figure 11-2. QPI Read ID (MR Read 'hB5)

Table 11-1. Known Good Die (KGD)

KDG[7:0]	KGD
'b0101_0101	Fail
'b0101_1101	Pass

> 📖 **Note:**
>
> Default is FAIL die, and only mark PASS after all tests passed.

12. Input/OutputTiming

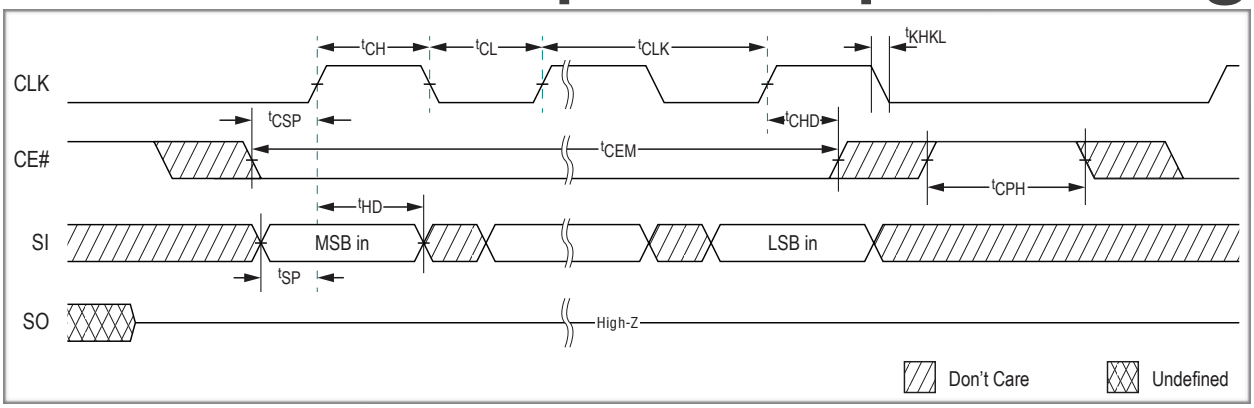


Figure 12-1. Input Timing

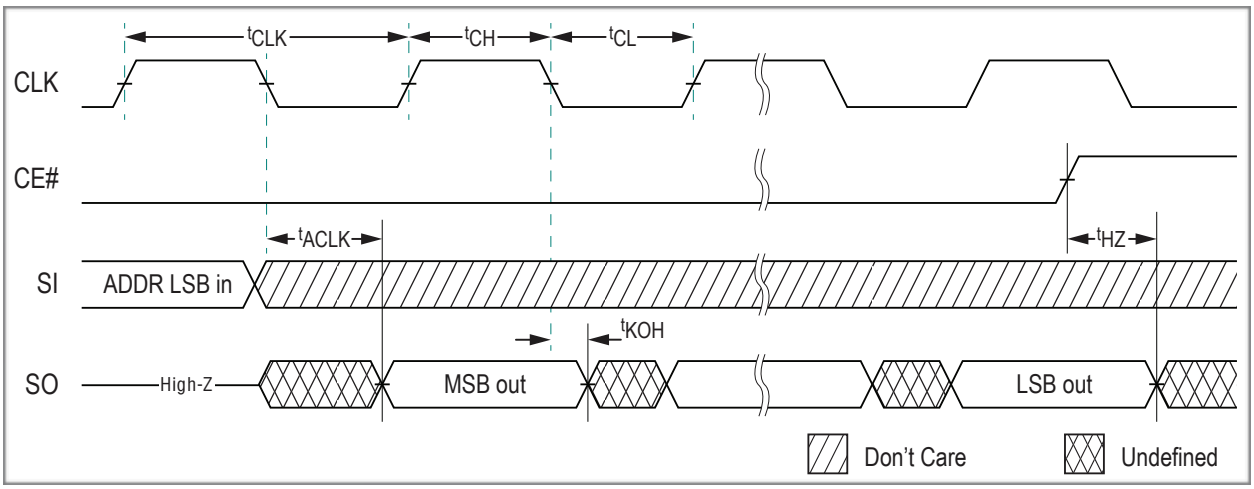


Figure 12-2. Output Timing

13. Electrical Specifications

> ⚠ **Notice:**
>
> Exposing the device to stress greater than the listed Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits specified in this document. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

13.1. Absolute Maximum Ratings

Table 13-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VT	Voltage to any pad except V_{DD} relative to Vss	–0.4 ~ V_{DD} +0.4	V
V_{DD}	Voltage on V_{DD} relative to Vss	–0.4 ~ +4.0	V
T_{STG}	Storage Temperature *	–55 ~ +150	°C

> 📖 **Note:**
>
> * Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

13.2. Operating Conditions

Table 13-2. Operating Conditions

Parameter	Min	Max	Unit
Operating Temperature	–40	85	°C

13.3. Pin Capacitance

Table 13-3. Pin Capacitance

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Pin Capacitance	-	6	pF	V_{IN} = 0 V
C_{OUT}	Output Pin Capacitance	-	8	pF	V_{OUT} = 0 V

13.4. Load Capacitance

Table 13-4. Load Capacitance

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	-	20	pF

13.5. DC Electrical Characteristics

Table 13-5. DC Electrical Characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	2.7	3.6	V
V_{IH}	Input high voltage	V_{DD} – 0.4	V_{DD} + 0.3	V
V_{IL}	Input low voltage	–0.3	0.4	V
V_{OH}	Output high voltage (I_{OH} = –0.2 mA)	0.8 V_{DD}	-	V
V_{OL}	Output low voltage (I_{OL} = +0.2 mA)	-	0.2 V_{DD}	V
I_{LI}	Input leakage current	-	1	µA
I_{LO}	Output leakage current	-	1	µA
I_{CC}	Read/Write (133 MHz)	-	7	mA
	Read/Write (66 MHz)	-	6	mA
	Read/Write (13 MHz)	-	5	mA
I_{SB}	Standby current (standard room temp) *	-	40	µA

📖 **Note:**

* Standby current is measured when CLK is in DC low state.

13.6. AC Electrical Characteristics

Table 13-6. AC Electrical Characteristics

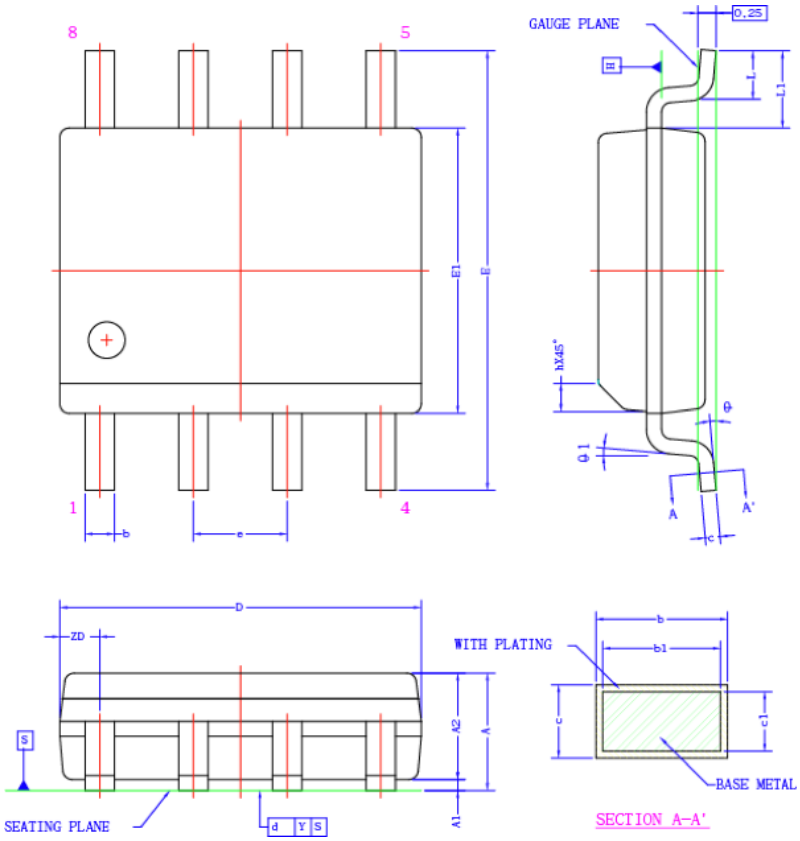
Symbol	Parameter	Min	Max	Unit	Notes
t_{CLK}	CLK period—SPI Read ('h03)	30.3	-	ns	33 MHz
	CLK period—QPI Read ('h0B)	15.1			66 MHz
	CLK period - all other operations (3 V)	7.5			133 MHz note 1
	CLK period - all other operations (3.3 V)	9.17			109 MHz

Symbol	Parameter	Min	Max	Unit	Notes
t_{CH}/t_{CL}	Clock high/low width	0.45	0.55	t_{CLK} (min)	-
t_{KHKL}	CLK rise or fall time	-	1.5	ns	note 2
t_{CPH}	CE# HIGH between subsequent burst operations	18	-	ns	-
t_{CEM}	CE# low pulse width	-	8	µs	-
t_{CSP}	CE# setup time to CLK rising edge	2.5	-	ns	-
t_{CHD}	CE# hold time from CLK rising edge	3	-	ns	-
t_{SP}	Setup time to active CLK edge	2	-	ns	-
t_{HD}	Hold time from active CLK edge	2	-	ns	-
t_{HZ}	Chip disable to DQ output hight-Z	-	5.5	ns	-
t_{ACLK}	CLK to output delay	2	5.5	ns	note 2
t_{KOH}	Data hold time from clock falling edge	1.5	-	ns	-
t_{RST}	Time between end of RST CMD to next valid CMD	50	-	ns	-

📖 **Notes:**

1. For operating frequencies >84 MHz, it is highly recommended to utilize CLK falling edge to sample read data or align sampling clock via data pattern tuning (refer to JEDEC JESD84-B50 for an example).
2. Measured from 20% to 80% of V_{DD}.

14. Product Outline Dimensions



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	1.75	53	63	69
A1	0.10	0.15	0.25	4	6	10
A2	1.35	1.45	1.55	53	57	61
b	0.31	–	0.51	12	–	20
b1	0.28	0.40	0.48	11	16	19
c	0.17	–	0.25	7	–	10
c1	0.17	0.20	0.23	7	8	9
D	4.80	4.90	5.00	189	193	197
E	6.00 BSC			236 BSC		
E1	3.80	3.90	4.00	150	154	157
e	1.27 BSC			50 BSC		
L	0.40	0.66	1.27	16	26	50
L1	1.05 REF			41 REF		
ZD	0.55 REF			22 REF		
h	0.25	0.38	0.50	10	15	20
Y	–	–	0.10	–	–	4
θ	0°	–	8°	0°	–	8°
θ1	0°	–	–	0°	–	–

NOTE :

1. REFER TO JEDEC STD: MS-012 AA.
2. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
   DIMENSION "E1" DOES NOT INCLUDE INTERLEAD MOLD FLASH OR PROTRUSION. INTERLEAD MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25mm PER SIDE.
   'D' AND 'E1' DIMENSIONS ARE DETERMIND AT DATUM H .
3. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE 'b' DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

A. Appendix–Device Marking Convention

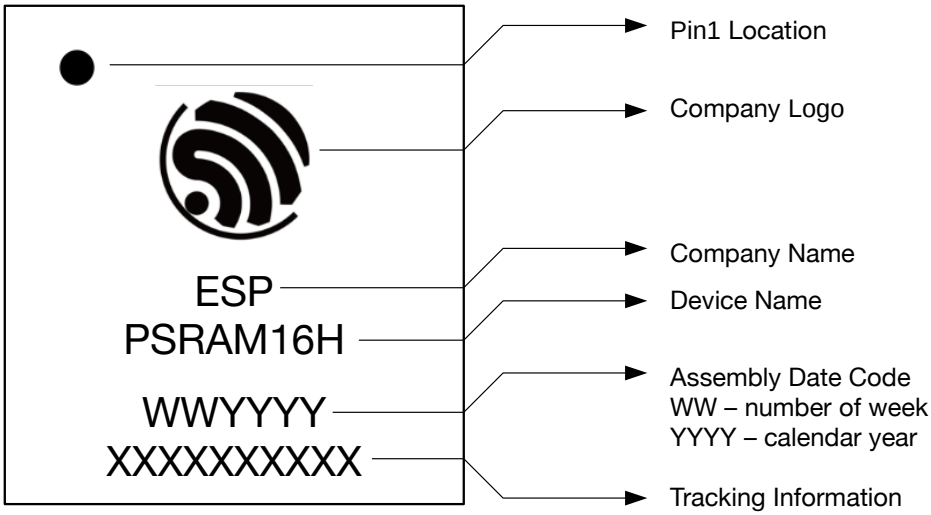


Figure A-1. Device Marking of ESP-PSRAM16H

📖 **Note:**

The content and the number of digits of the Tracking Information are subject to change.

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