ESP32-H2 Series SoC

Errata

Introduction

This document describes known errata in ESP32-H2 series of SoCs.

Version 0.5
Espressif Systems

Contents

Chip Identification

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/sites/default/files/documentation/esp32-h2_errata_en.pdf

1 Chip Revision

Espressif is introducing **vM.X** numbering scheme to indicate chip revisions.

M – Major number, indicating the major revision of the chip product. If this number changes, it means the software used for the previous version of the product is incompatible with the new product, and the software version shall be upgraded for the use of the new product.

X – Minor number, indicating the minor revision of the chip product. If this number changes, it means the software used for the previous version of the product is compatible with the new product, and there is no need to upgrade the software.

The vM.X scheme replaces previously used chip revision schemes, including ECOx numbers, Vxxx, and other formats if any.

The chip revision is identified by:

- eFuse field EFUSE_RD_MAC_SYS_3_REG[22:21] and EFUSE_RD_MAC_SYS_3_REG[20:18]

Table 1: Chip Revision Identification by eFuse Bits

	eFuse Bit	Chip Revision	
		v0.0	v0.1
Major Number	EFUSE_RD_MAC_SYS_3_REG[22]	0	0
	EFUSE_RD_MAC_SYS_3_REG[21]	0	0
Minor Number	EFUSE_RD_MAC_SYS_3_REG[20]	0	0
	EFUSE_RD_MAC_SYS_3_REG[19]	0	0
	EFUSE_RD_MAC_SYS_3_REG[18]	0	1

- **Espressif Tracking Information** line in chip marking

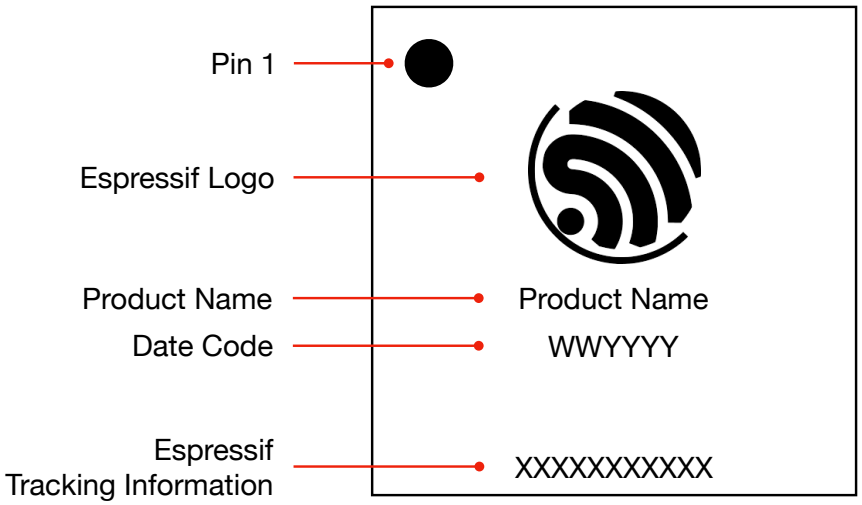

Figure 1: Chip Marking Diagram

Table 2: Chip Revision Identification by Silk Print

Chip Revision	Espressif Tracking Information
v0.0	XAXXXXXXX
v0.1	XBXXXXXXX

- **Specification Identifier** line in module marking

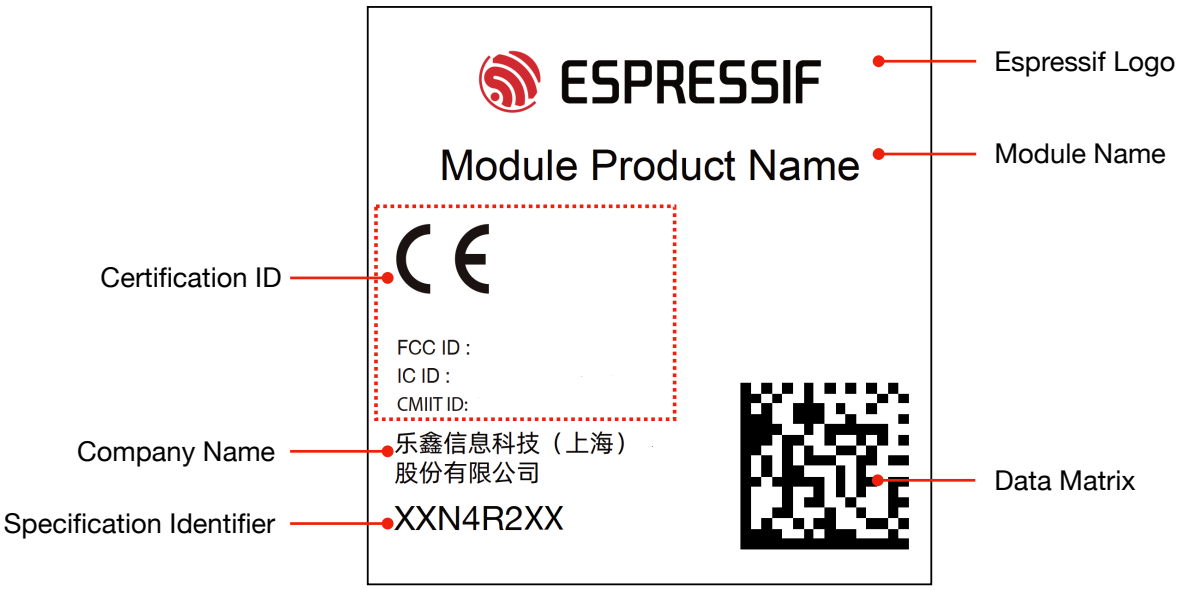

Figure 2: Module Marking Diagram

Table 3: Chip Revision Identification by Module Marking

Chip Revision	Specification Identifier[1]
v0.0	—
v0.1	MBXXXX

[1] "—" in this column means modules with this chip revision are not mass produced.

Note:

- Information about ESP-IDF release that supports a specific chip revision is provided in Compatibility Between ESP-IDF Releases and Revisions of Espressif SoCs.
- For more information about the chip revision upgrade and their identification of ESP32-H2 series products, please refer to ESP32-H2 Product/Process Change Notifications (PCN).
- For more information about the chip revision numbering scheme, see Compatibility Advisory for Chip Revision Numbering Scheme.

2 Additional Methods

Some errors in the chip product don't need to be fixed at the silicon level, or in other words in a new chip revision.

In this case, the chip may be identified by **Date Code** in chip marking (see Figure 1). For more information, please refer to *Espressif Chip Packaging Information*.

Modules built around the chip may be identified by **PW Number** in product label (see Figure 3). For more information, please refer to *Espressif Module Packaging Information*.

Figure 3: Module Product Label

Note:

Please note that **PW Number** is only provided for reels packaged in aluminum moisture barrier bags (MBB).

Errata Description

Table 4: Errata Summary

Category	Description	Affected Revisions	
		v0.0	v0.1
RISC-V CPU	3.1 *Out-of-order Execution of HP CPU when Compiling Codes in LP SRAM*	Y	Y
ADC	4.1 *Unavailable Channel 4 in ADC1*	Y	Y
Clocks	5.1 *Inaccurate Calibration of RC_FAST_CLK Clock*	Y	Y

3 RISC-V CPU

3.1 Out-of-order Execution of HP CPU when Compiling Codes in LP SRAM

Description

When HP CPU executes instructions (instruction A and instruction B successively) in LP SRAM, and instruction A and instruction B happen to follow the following patterns:

- Instruction A involves writing to memory. Examples: **sw**/**sh**/**sb**
- Instruction B involves only accessing the instruction bus. Examples: **nop**/**jal**/**jalr**/**lui**/**auipc**
- The address of instruction B is not 4-byte aligned

The data written by instruction A to memory is only committed after instruction B has completed execution. This introduces a risk where, after instruction A writing to memory, if an infinite loop is executed in instruction B, the writing of instruction A will never complete.

Workarounds

- Add a **fence** instruction between instruction A and the infinite loop. This can be achieved by using the *rv_utils_memory_barrier* interface in ESP-IDF.
- Replace the infinite loop with instruction **wfi**. This can be achieved by using the *rv_utils_wait_for_intr* interface in ESP-IDF.
- Disable the RV32C (compressed) extension when compiling code that to be executed in LP SRAM to avoid instructions with not 4-byte aligned addresses.

Projected Solution

To be fixed in the future chip revisions.

4 Analog-to-Digital Converter (ADC)

4.1 Unavailable Channel 4 in ADC1

Description

Channel 4 (ADC1_CH4) of ADC1 is not operational in chip revision v0.1.

Workarounds

Use other channels instead of ADC1_CH4.

Projected Solution

To be fixed in the next chip revision.

5 Clocks

5.1 Inaccurate Calibration of RC_FAST_CLK Clock

Description

In the ESP32-H2 chip version v0.1, the frequency of the RC_FAST_CLK clock source is too close to the reference clock (32 MHz XTAL_CLK) frequency, making it impossible to calibrate accurately. This may affect peripherals that rely on RC_FAST_CLK and have stringent requirements for its accurate clock frequency.

Workarounds

Use other clock sources instead of RC_FAST_CLK.

Projected Solution

To be fixed in the next chip revision.

Related Documentation and Resources

Related Documentation

- ESP32-H2 Series Datasheet – Specifications of the ESP32-H2 hardware.
- ESP32-H2 Technical Reference Manual – Detailed information on how to use the ESP32-H2 memory and peripherals.
- ESP32-H2 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-H2 into your hardware product.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-H2 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-H2
- *ESP32-H2 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-H2
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-H2 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-H2 Series SoCs* – Browse through all ESP32-H2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-H2
- *ESP32-H2 Series Modules* – Browse through all ESP32-H2-based modules.
  https://espressif.com/en/products/modules?id=ESP32-H2
- *ESP32-H2 Series DevKits* – Browse through all ESP32-H2-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-H2
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

Contact Us

- See the tabs *Sales Questions*, *Technical Enquiries*, *Circuit Schematic & PCB Design Review*, *Get Samples* (Online stores), *Become Our Supplier*, *Comments & Suggestions*.
  https://espressif.com/en/contact-us/sales-questions

Revision History

Date	Version	Release Notes
2023-10-17	v0.5	First release

www.espressif.com

Disclaimer and Copyright Notice