ESP32-S2 Series SoC

Errata

Introduction

This document describes known errata in ESP32-S2 series of SoCs.

Version 1.0

Espressif Systems

Contents

Chip Revision Identification

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/sites/default/files/documentation/esp32-s2_errata_en.pdf

The chip revision is identified by:

- eFuse field EFUSE_RD_MAC_SPI_SYS_3_REG[20:18] and EFUSE_RD_MAC_SPI_SYS_4_REG[6:4]

Table 1: Chip Revision Identification by eFuse Bits

	eFuse Bit	Chip Revision	
		v0.0	v1.0
Major Number	EFUSE_RD_MAC_SPI_SYS_3_REG[19]	0	0
	EFUSE_RD_MAC_SPI_SYS_3_REG[18]	0	1
Minor Number	EFUSE_RD_MAC_SPI_SYS_3_REG[20]	0	0
	EFUSE_RD_MAC_SPI_SYS_4_REG[6]	0	0
	EFUSE_RD_MAC_SPI_SYS_4_REG[5]	0	0
	EFUSE_RD_MAC_SPI_SYS_4_REG[4]	0	0

- **Main Die** line in chip marking

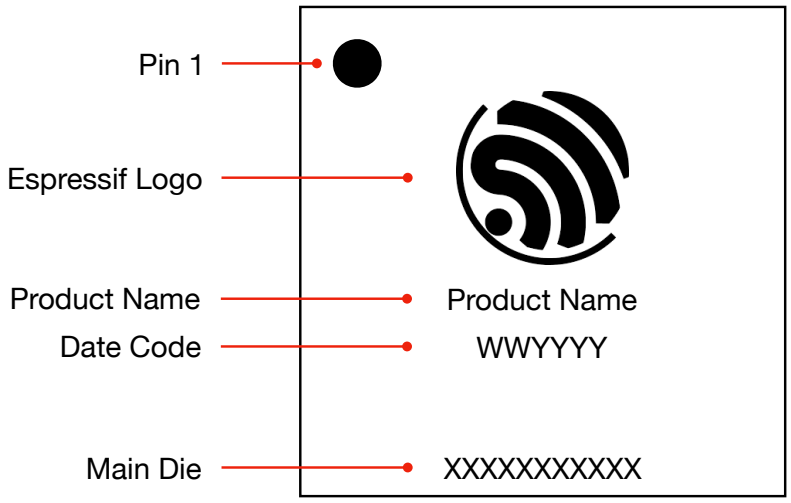

Figure 1: Chip Marking Diagram

Table 2: Chip Revision Identification by Silk Print

Chip Revision	Main Die
v0.0	XAXXXXXXX
v1.0	XBXXXXXXX

Note:

Information about ESP-IDF release that supports a specific chip revision is provided in ESP Product Selector.

Errata Description

Table 3: Errata Summary

Category	Description	Affected Revisions	
		v0.0	v1.0
System	1.1 *Leakage current at the VDDA and VDD3P3_RTC pin during shutdown*	Y	
	1.2 *Random flash download failure*	Y	
RTC I2C	2.1 *The falling edge of RTC_I2C_RESET triggers reset at low temperature*	Y	
SPI	3.1 *SPI is stuck after soft restart from auto suspension*	Y	
USB OTG	4.1 *Abnormal data during AHB bus arbitration by USB OTG*	Y	
SAR ADC	5.1 *Bit 1 of SAR ADC does not flip*	Y	

1 System

1.1 Leakage current at the VDDA and VDD3P3_RTC pin during shutdown

Description

When a chip is connected to the power supply, but the CHIP_PU pin is held low (meaning that the chip powers off), there will be a leakage current in the μA range at power pins such as VDDA and VDD3P3_RTC.

Workarounds

No.

Projected Solution

Fixed in chip revision v1.0.

1.2 Random flash download failure

Description

In download mode, the first stage bootloader in ROM receives serial data from two different input pins. Among the two intput pins, pin 24 DAC_2 (GPIO18) is not pulled up by default. If this pin is not pulled up in PCB design and is left floating, in download mode the first stage bootloader will not function properly (including download applications) due to interference.

Workarounds

This problem can be bypassed in PCB design by pulling up pin 24 DAC_2. The typical value of the pull-up resistor is 10 kΩ. All official development boards by Espressif pull this pin up, while official modules are not.

Projected Solution

Fixed in chip revision v1.0 by pulling pin 24 up by default.

2 RTC I2C

2.1 The falling edge of RTC_I2C_RESET triggers reset at low temperature

Description

At –40 °C, the chip will be restarted during wake-up.

Workarounds

No.

Projected Solution

Fixed in chip revision v1.0.

3 SPI

3.1 SPI is stuck after soft restart from auto suspension

Description

After auto suspend is enabled, if caching is requested while Memory SPI is erasing flash, Memory SPI will automatically send a SUSPEND command (0x75). If there is a system reset, and Memory SPI is restarted before sending a RESUME command (0x7A), the state machine of Memory SPI will not be restored. As a result, the system cannot continue operations.

Workarounds

Disable auto suspend function.

Projected Solution

Fixed in chip revision v1.0.

4 USB OTG

4.1 Abnormal data during AHB bus arbitration by USB OTG

Description

When USB OTG and other peripherals on ESP32-S2 request the AHB bus at the same time, the AHB bus might generate wrong arbitration signals, which result in abnormal data during reads and writes by USB OTG. The competing peripherals include:

- I2S
- SPI

Workarounds

1. Avoid AHB bus competition between USB OTG and above peripherals by not using DMA mode of USB OTG, or disabling DMA mode of above peripherals.
2. Avoid interrupt while USB OTG is using the AHB bus. Specifically, set USB OTG's AHB burst transfer to INCR mode. In this mode, USB OTG will occupy the AHB bus exclusively until the burst transfer is completed.

> **Note:**
> Use the second workaround with care, as it requires adjustment to maximum packet size (MPS) for USB OTG endpoints, so that burst time is smaller than the timeout period of the competing peripherals.

Projected Solution

Fixed in chip revision v1.0.

5 SAR ADC

5.1 Bit 1 of SAR ADC does not flip

Description

Bit 1 of SAR ADC is always 0, and does not change with measured voltage.

Workarounds

No.

Projected Solution

Fixed in chip revision v1.0. The effective resolution of SAR ADC on chip revision v1.0 is changed from 13 bits to 12 bits. That is, bit 0 is not valid, and the valid bits are bit 1 ~ bit 12 inclusive.

Related Documentation and Resources

Related Documentation

- ESP32-S2 Series Datasheet – Specifications of the ESP32-S2 hardware.
- ESP32-S2 Technical Reference Manual – Detailed information on how to use the ESP32-S2 memory and peripherals.
- ESP32-S2 Hardware Design Guidelines – Guidelines on how to integrate the ESP32-S2 into your hardware product.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S2 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns
- *ESP32-S2 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S2 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S2 Series SoCs* – Browse through all ESP32-S2 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S2
- *ESP32-S2 Series Modules* – Browse through all ESP32-S2-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S2
- *ESP32-S2 Series DevKits* – Browse through all ESP32-S2-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S2
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Revision History

Date	Version	Release Notes
2022-09-19	v1.0	First release

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