ESP32-S3 Series

Hardware Design Guidelines

Introduction

Hardware design guidelines give advice on how to integrate ESP32-S3 into other products. ESP32-S3 is a series of high-performance Wi-Fi and Bluetooth® 5 (LE) SoCs.

These guidelines will help to ensure optimal performance of your product with respect to technical accuracy and conformity to Espressif's standards.

Version 1.2

Espressif Systems

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1 Overview

Note:

Check the link or the QR code to make sure that you use the latest version of this document:
https://espressif.com/documentation/esp32-s3_hardware_design_guidelines_en.pdf

ESP32-S3 is a highly-integrated, low-power, 2.4 GHz Wi-Fi + Bluetooth® LE (5) System-on-Chip (SoC) solution. It has the following features:

- Xtensa® 32-bit LX7 CPU operating at clock speeds up to 240 MHz
- Complete Wi-Fi + Bluetooth subsystem integrating radio and baseband, RF switch, RF balun, power amplifier, low noise amplifier (LNA), etc
- State-of-the-art power management unit
- Industry-leading RF performance
- Powerful AI computing ability
- Rich set of peripherals

ESP32-S3 also integrates advanced calibration circuitry that compensates for radio imperfections, and thus reduces the cost and time to the market for your product, and eliminates the need for specialized testing equipment.

The SoC is an ideal choice for a wide variety of application scenarios related to AI and Artificial Intelligence of Things (AIoT), such as:

- Wake word detection
- Speech commands recognition
- Face detection and recognition
- Smart home
- Smart appliances
- Smart control panel
- Smart speaker

For more information about ESP32-S3 series, please refer to *ESP32-S3 Series Datasheet*.

Note:

Unless otherwise specified, "ESP32-S3" used in this document refers to ESP32-S3 chips without in-package flash/P-SRAM.

2 Schematic Checklist

The integrated circuitry of ESP32-S3 requires only about 20 electrical components (resistors, capacitors, and inductors), one crystal and one SPI flash memory chip. The high integration of ESP32-S3 allows for simple peripheral circuit design. This chapter details ESP32-S3 schematics.

ESP32-S3 schematic is shown in Figure 1.

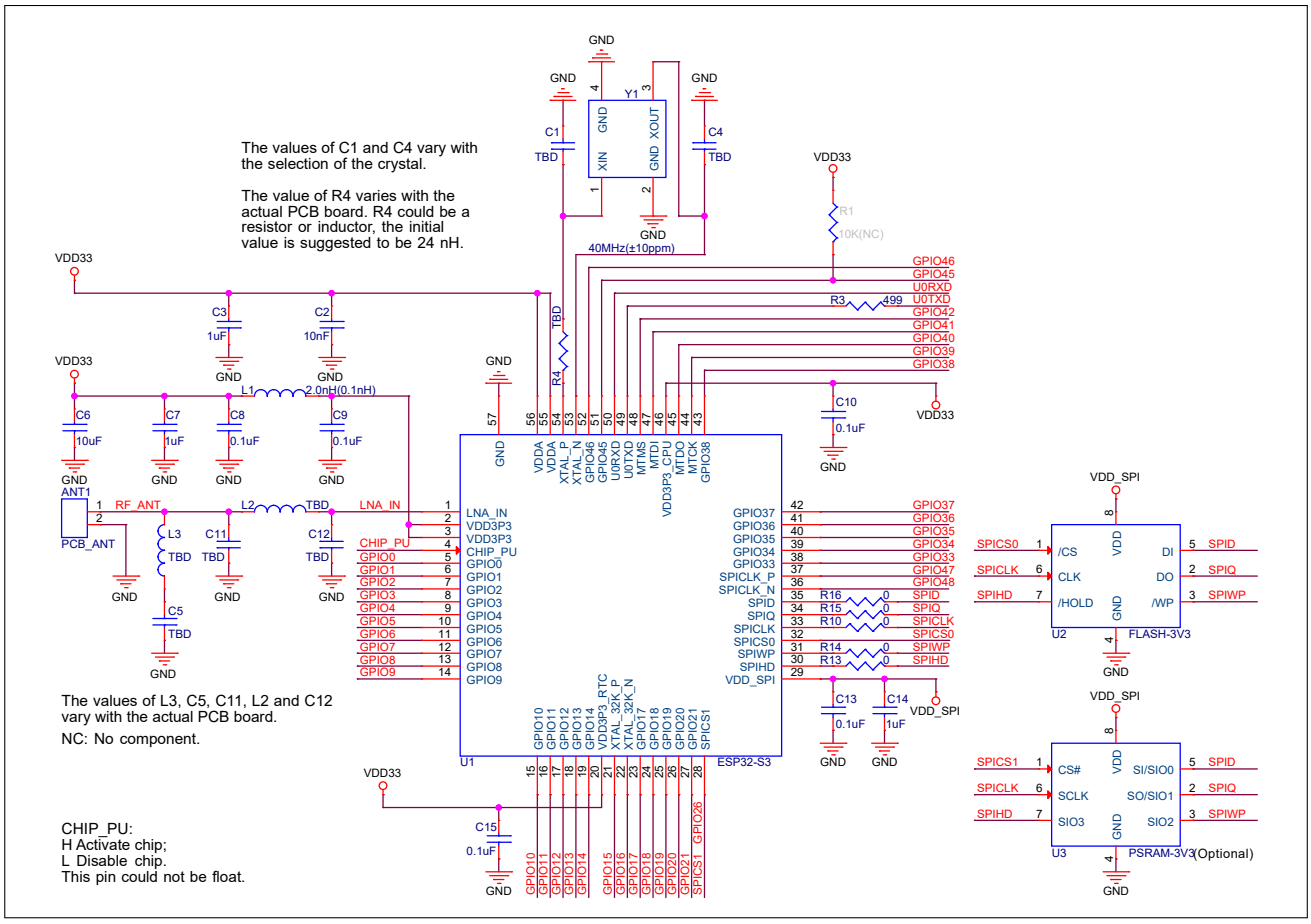

Figure 1: ESP32-S3 Schematic

Notice:

Figure 1 shows the connection for 3.3 V, quad, off-package SPI flash/PSRAM.

In cases where 1.8 V or 3.3 V, octal, in-package or off-package SPI flash/PSRAM is used, GPIO33 ~ GPIO37 are occupied and cannot be used for other functions.

In cases where in-package SPI flash/PSRAM is used, VDD_SPI is fixed to 1.8 V or 3.3 V, then GPIO45 will not affect any more. In other cases, choose whether to populate R1 according to Table 1.

The connection for 1.8 V, octal, off-package flash/PSRAM is as shown in Figure 2.

When only in-package flash/PSRAM is used, there is no need to populate the resistor on the SPI traces or to care the SPI traces.

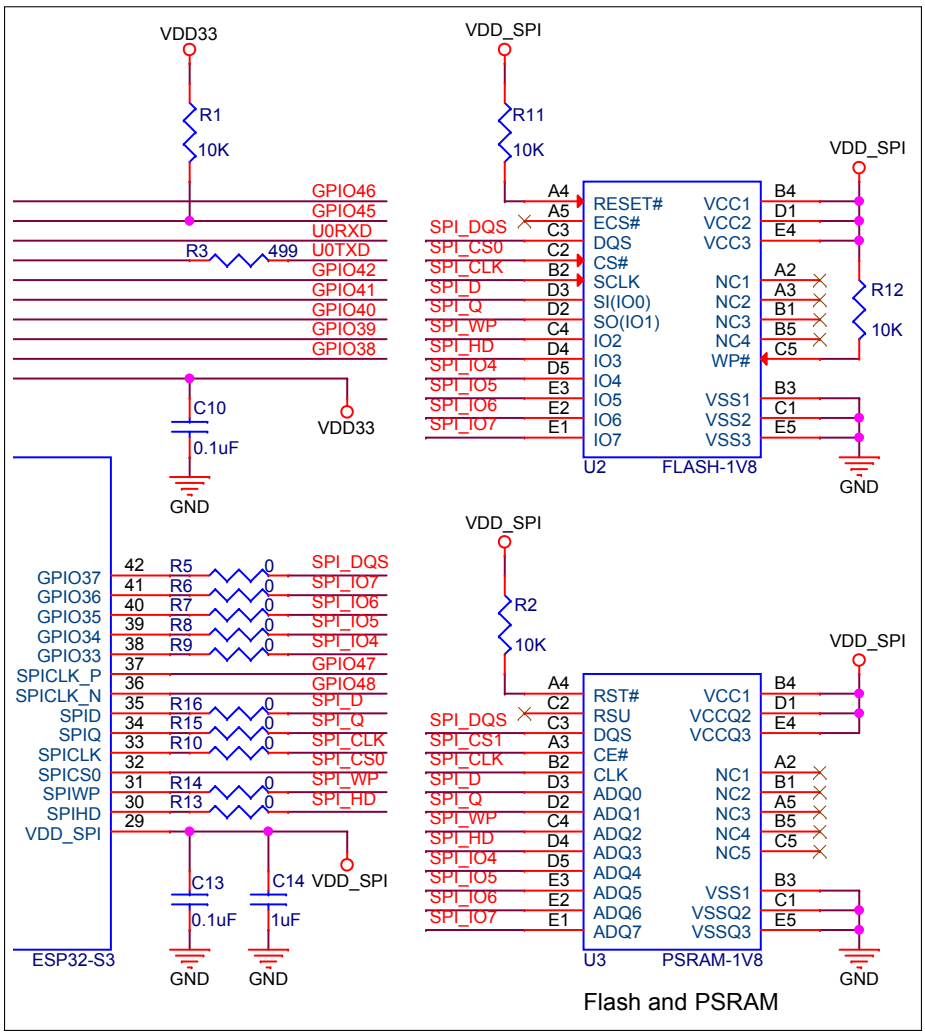

Figure 2: ESP32-S3 Schematic for the Off-Package Octal Flash/PSRAM (1.8 V)

Any basic ESP32-S3 circuit design may be broken down into 12 major sections:

- Power supply
- Power-on sequence and system reset
- Flash and SRAM
- Clock source
- RF
- UART
- Strapping pins
- GPIO
- ADC
- USB
- SDIO
- Touch sensor

The rest of this document details the specifics of circuit design for each of these sections.

2.1 Power Supply

Details of using power supply pins can be found in Section *Power Scheme* in *ESP32-S3 Series Datasheet*.

2.1.1 Digital Power Supply

Pin46 VDD3P3_CPU of ESP32-S3 supplies power to CPU IO with a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 μF decoupling capacitor close to VDD3P3_CPU.

Pin29 VDD_SPI can serve as the power supply output at either 1.8 V or 3.3 V (default). It is recommended to add extra 0.1 μF and 1 μF decoupling capacitors close to VDD_SPI.

- When VDD_SPI operates at 1.8 V, it is powered by the internal flash voltage regulator on the chip. The typical current the flash voltage regulator can offer is 40 mA.
- When VDD_SPI operates at 3.3 V, it is driven directly by VDD3P3_RTC through the internal R_{SPI} resistor with a typical value of 14 Ω. Therefore, there will be some voltage drop from VDD3P3_RTC.

Depending on the value of EFUSE_VDD_SPI_FORCE, the VDD_SPI voltage of ESP32-S3 can be controlled in two ways.

Table 1: VDD_SPI Voltage Control

EFUSE_VDD_SPI_FORCE	GPIO45	eFuse [1]	Voltage	VDD_SPI power source [2]
0	0	Ignored	3.3 V	VDD3P3_RTC via R_{SPI}
	1		1.8 V	Flash Voltage Regulator
1	Ignored	0	1.8 V	Flash Voltage Regulator
		1	3.3 V	VDD3P3_RTC via R_{SPI}

[1] eFuse: EFUSE_VDD_SPI_TIEH
[2] See *ESP32-S3 Series Datasheet* > Section *Power Scheme*

VDD_SPI can also be the power supply input driven by an external power supply.

Notice:

- For ESP32-S3 chips with in-package flash/PSRAM, VDD_SPI is fixed to 1.8 V or 3.3 V, so it is not required to configure GPIO45.
- When using VDD_SPI as the power supply output for in-package or off-package 3.3 V flash/PSRAM, considering a voltage drop due to the R_{SPI} resistor, VDD3P3_RTC is suggested to be 3.0 V or above to meet the flash/PSRAM's minimum working voltage requirement.

The schematic for the digital power supply pins is shown in Figure 3.

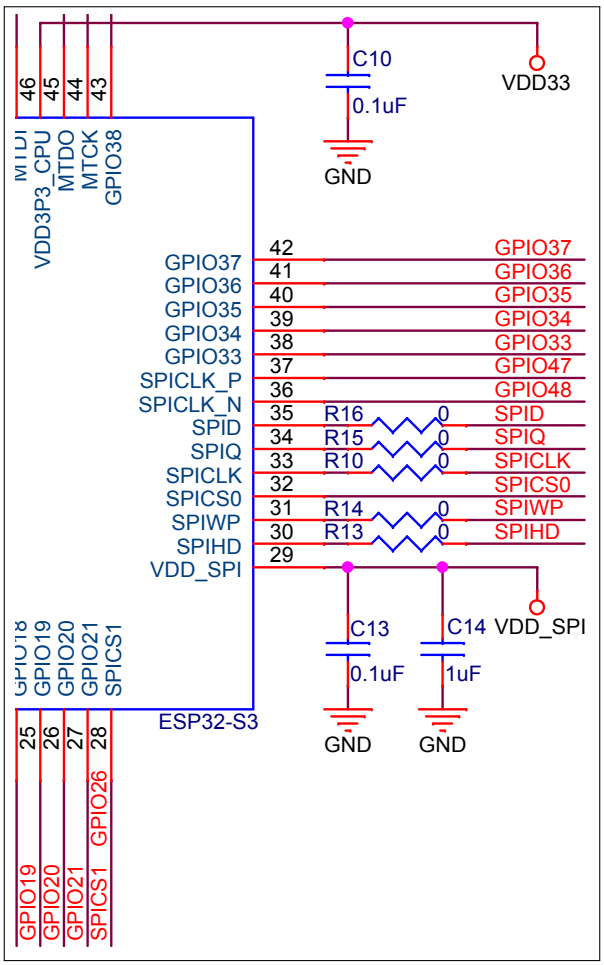

Figure 3: Schematic for the Digital Power Supply Pins

2.1.2 Analog Power Supply

Pin2 VDD3P3, pin3 VDD3P3, pin55 VDDA, and pin56 VDDA are the analog power supply pins working at 3.0 V ~ 3.6 V.

Please be noted that the sudden increase in current draw, when ESP32-S3 is transmitting signals, may cause a power rail collapse. Therefore, it is highly recommended to add a 10 μF capacitor to the power pin2 and power pin3 VDD3P3, which can work in conjunction with the 1 μF capacitor. In addition, a CLC filter circuit needs to be added near VDD3P3 pins so as to suppress high-frequency harmonics. The recommended rated current of the inductor is 500 mA or above. Refer to Figure 4 to place the appropriate decoupling capacitors near each analog power pin.

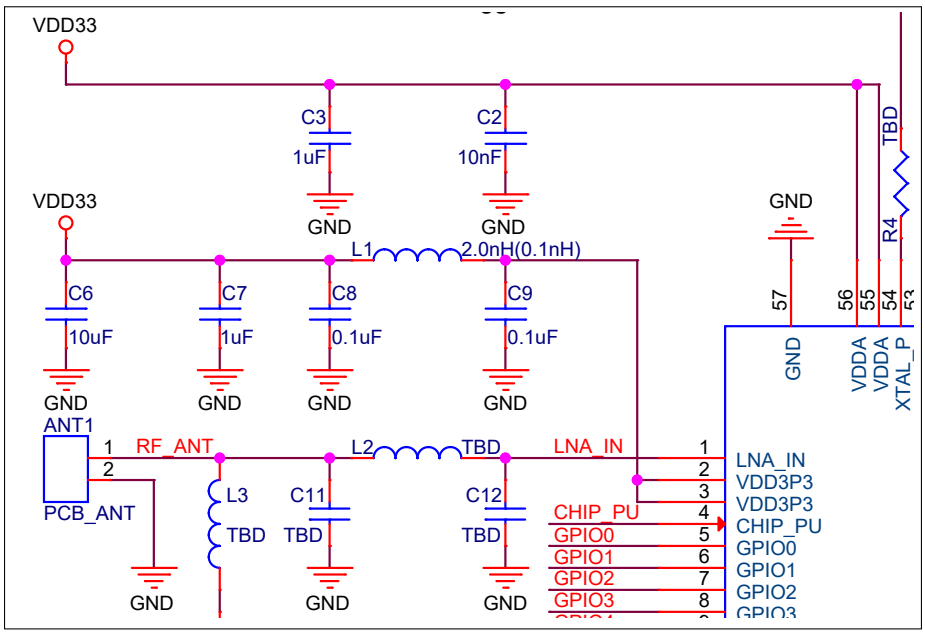

Figure 4: Schematic for the Analog Power Supply Pins

2.1.3 RTC Power Supply

Pin20 VDD3P3_RTC of ESP32-S3 series chips supplies power to the RTC part. It is recommended to place a 0.1 μf decoupling capacitor near this power pin in the circuit.

Note that this power supply cannot be used as the single backup power supply.

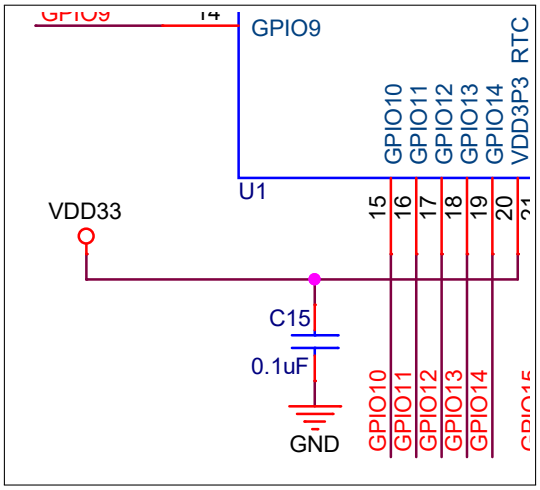

Figure 5: ESP32-S3 RTC Power Supply

Notice:

- When using a single power supply for ESP32-S3, the recommended power supply voltage is 3.3 V and the output current should be no less than 500 mA.
- It is suggested to add another 10 μF capacitor at the power entrance. If the power entrance is close to pin2 and pin3, it can share the same 10 μF capacitor with pin2 and pin3.
- It is suggested to add an ESD protection diode at the power entrance.

2.2 Power-up Timing and System Reset

2.2.1 Power-up Timing

When ESP32-S3 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_PU is pulled up and the chip is enabled. Therefore, CHIP_PU needs to be powered up after the 3.3 V rails have been brought up. More details about the power-up timing can be found in Section 2.2.3.

Notice:

To ensure the correct power-up timing, it is advised to add an RC delay circuit at the CHIP_PU pin. The recommended setting for the RC delay circuit is usually R = 10 kΩ and C = 1 μF. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing sequence of the chip.

2.2.2 System Reset

CHIP_PU serves as the reset pin of ESP32-S3. When CHIP_PU is at low level, the reset voltage (V_{IL_nRST}) should be in the range of (–0.3 ~ 0.25 × VDD3P3_RTC) V. To avoid reboots caused by external interferences, make the CHIP_PU trace as short as possible. Also, add a pull-up resistor as well as a capacitor to ground whenever possible. More details can be found in Section 2.2.3.

Notice:

CHIP_PU pin must not be left floating.

2.2.3 Power-up and Reset Timing

Figure 6 shows the power-up and reset timing of ESP32-S3 series of chips. Details about the parameters are listed in Table 2.

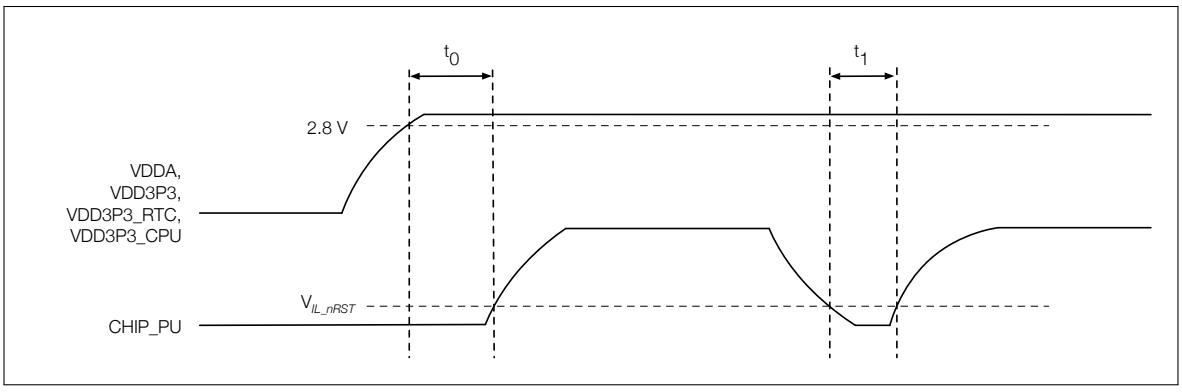

Figure 6: ESP32-S3 Power-up and Reset Timing

Table 2: Description of ESP32-S3 Power-up and Reset Timing Parameters

Parameter	Description	Min (μs)
t_0	Time between bringing up the power rails of VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU and activating CHIP_PU	50
t_1	Duration of CHIP_PU signal level < V_{IL_nRST} to reset the chip	50

Notice:

In cases where the power supply ramps up slowly (e.g., during battery charging), or the device needs to be frequently powered on and off, or the power supply is unstable (e.g., in solar photovoltaic systems), adding a single RC circuit might not meet the requirements for power-up and reset timing, and consequently the chip will not boot correctly. In this case, it is advised to take other approaches, such as adding an external reset chip or a watchdog timer IC. If VDD_SPI operates at 3.3 V output mode, the threshold of reset chip or watchdog timer IC is suggested to be around 3.0 V.

2.3 Flash and SRAM

ESP32-S3 requires in-package or off-package flash to store application firmware and data. In-package PSRAM or off-package RAM is optional.

2.3.1 In-Package Flash/PSRAM

In-package flash/PSRAM refer to the flash and PSRAM that is integrated into the package of a specific chip variant. For the pin-to-pin mapping between the chip and in-package flash/PSRAM, please refer to Table 3.

Please note that the following pins can connect at most one flash and one PSRAM. That is to say, when there is only flash in the package, the pin occupied by flash can only connect PSRAM and cannot be used for other functions; when there is only PSRAM, the pin occupied by PSRAM can only connect flash; when there are both flash and PSRAM, the pin will be unavailable.

2.3.2 Pin-to-Pin Mapping Between Chip and In-Package Flash/PSRAM

Table 3 lists the pin-to-pin mapping between the chip and the in-package flash/PSRAM. The chip pins listed here are not recommended for other usage.

Table 3: Pin-to-Pin Mapping Between Chip and In-Package Flash/PSRAM

ESP32-S3FN8 (8 MB) / ESP32-S3FH4R2 (4 MB)	In-Package Flash (Quad SPI)
SPICLK	CLK
SPICS0	CS#
SPID	DI
SPIQ	DO
SPIWP	WP#
SPIHD	HOLD#
ESP32-S3R2 / ESP32-S3FH4R2	**In-Package PSRAM (2 MB, Quad SPI)**
SPICLK	CLK
SPICS1	CE#
SPID	SI/SIO0
SPIQ	SO/SIO1
SPIWP	SIO2
SPIHD	SIO3
ESP32-S3R8 / ESP32-S3R8V	**In-Package PSRAM (8 MB, Octal SPI)**
SPICLK	CLK
SPICS1	CE#

SPID	DQ0
SPIQ	DQ1
SPIWP	DQ2
SPIHD	DQ3
GPIO33	DQ4
GPIO34	DQ5
GPIO35	DQ6
GPIO36	DQ7
GPIO37	DQS/DM

2.3.3 Off-Package Flash/PSRAM

ESP32-S3 supports up to 1 GB off-package flash and 1 GB off-package RAM. If VDD_SPI is used to supply power, make sure to select the appropriate off-package flash and RAM according to the power voltage on VDD_SPI (1.8 V/3.3 V). It is recommended to add a zero-ohm series resistor on the SPI communication lines to lower the driving current, reduce interference to RF, adjust timing, and better shield from interference.

The ESP32-S3 schematics respectively for the off-package quad flash/PSRAM and off-package octal flash/PSRAM are shown in Figure 1 and Figure 2.

2.4 Clock Source

ESP32-S3 has two clock sources:

- External clock source
- RTC clock source

2.4.1 External Clock Source (Compulsory)

The ESP32-S3 firmware only supports 40 MHz crystal.

Crystal

The circuit for the crystal is shown in Figure 7. Note that the accuracy of the selected crystal should be within ±10 ppm.

Please add a series component (resistor or inductor, see R4 in Figure 7) on the XTAL_P clock trace. Initially, it is suggested to use an inductor of 24 nH to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be adjusted after an overall test.

The initial values of external capacitors C1 and C4 can be determined according to the formula:

$$C_L = \frac{C1 \times C4}{C1 + C4} + C_{stray}$$

where the value of C_L (load capacitance) can be found in the crystal's datasheet, and the value of C_{stray} refers to the PCB's stray capacitance. The values of C1 and C4 need to be further adjusted after an overall test as below:

1. Select TX tone mode using the Certification and Test Tool.

2. Observe the 2.4-GHz signal with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
3. Adjust the frequency offset to be within ±10 ppm (recommended) by adjusting the external load capacitance.
    - When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.
    - When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.
    - External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

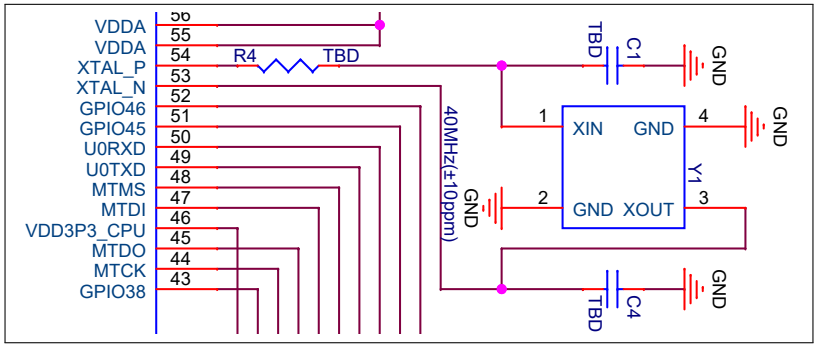

Figure 7: Schematic for the Crystal

Notice:

- Defects in the manufacturing of crystal and oscillators (for example, large frequency deviation of more than ±10 ppm, unstable performance within operating temperature range, etc) may lead to the malfunction of ESP32-S3, resulting in a decrease of the RF performance.
- It is recommended that the amplitude of the crystal is greater than 500 mV.
- When Wi-Fi or Bluetooth connection fails, after ruling out software problems, you may follow the steps mentioned above to ensure that the frequency offset meets the requirements by adjusting capacitors at the two sides of the crystal.

2.4.2 RTC (Optional)

ESP32-S3 supports an external 32.768 kHz crystal or an external signal (e.g., an oscillator) to act as the RTC sleep clock. The external RTC clock source is used to improve the timing accuracy and thus reduce the average power consumption, but will not affect the functionality.

Figure 8 shows the schematic for the external 32.768 kHz crystal.

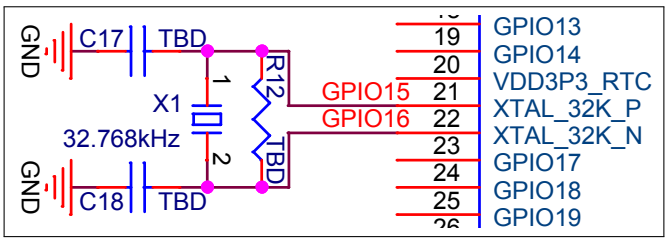

Figure 8: Schematic for the External Crystal (RTC)

Notice:

- Please note the requirements for the 32.768 kHz crystal.
  - Equivalent series resistance (ESR) $\leqslant 70\ k\Omega$.
  - Load capacitance at both ends should be configured according to the crystal's specification.
- The parallel resistor R is used for biasing the crystal circuit ($5\ M\Omega < R \leqslant 10\ M\Omega$). In general, you do not need to populate the resistor.
- If the RTC source is not required, then the pins for the external 32.768 kHz crystal can be used as other GPIOs.

Figure 9 shows the schematic of the external signal.

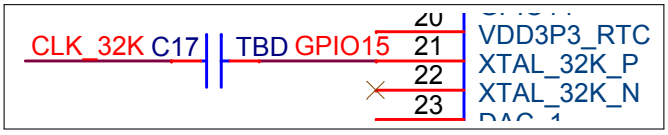

Figure 9: Schematic for ESP32-S3's External Oscillator (RTC)

The external signal can be input to the XTAL's P end through a DC blocking capacitor (about 20 pF). The XTAL's N end can be floating. The signal should meet the following requirements:

Input to XTAL's P End	Amplitude (Vpp, unit: V)
Sine wave or square wave	0.6 < Vpp < VDD

2.5 RF

The RF circuit of the ESP32-S3 series of chips is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna and the antenna matching circuit.

- For the RF traces on the PCB board, 50 Ω impedance control is required.
- For the chip matching circuit, it must be placed close to the chip. It is mainly used to adjust the impedance point and suppress harmonics. The CLC structure is preferred, and a set of LC can be added if space permits. The CLC matching circuit is shown in Figure 10.
- For the antenna and the antenna matching circuit, to ensure the radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

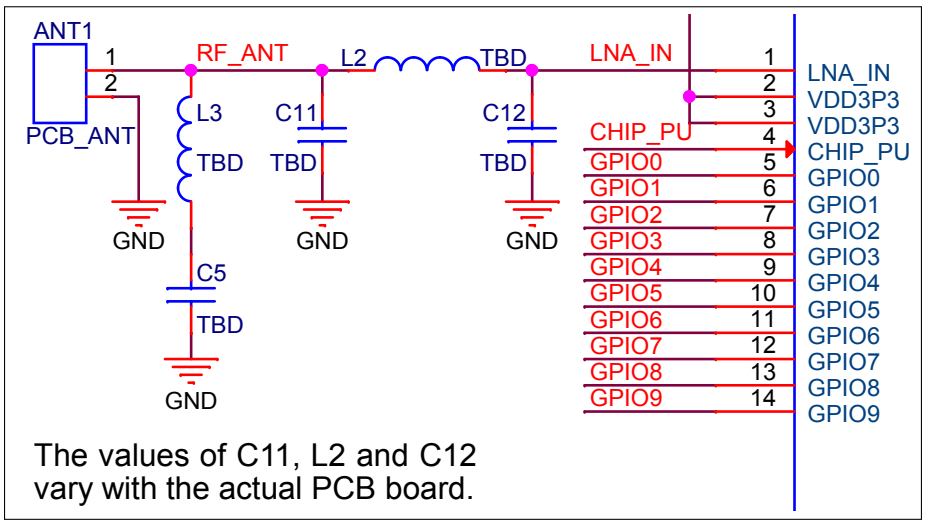

Figure 10: Schematic for RF Matching

Figure 11 shows the general process of RF tuning. Please be noted the matching parameters are subject to the RF tuning of PCB board, which depends greatly on the antenna and PCB layout. For ESP32-S3 series of chips, it is recommended to set the S11 parameter in the figure below to 35+j0 Ω and the center frequency is 2442 MHz.

If the RF function is not required, the RF pin can be left floating.

If the application or production environment is susceptible to electrostatic discharge, it is recommended to reserve an ESD protection diode near the antenna side.

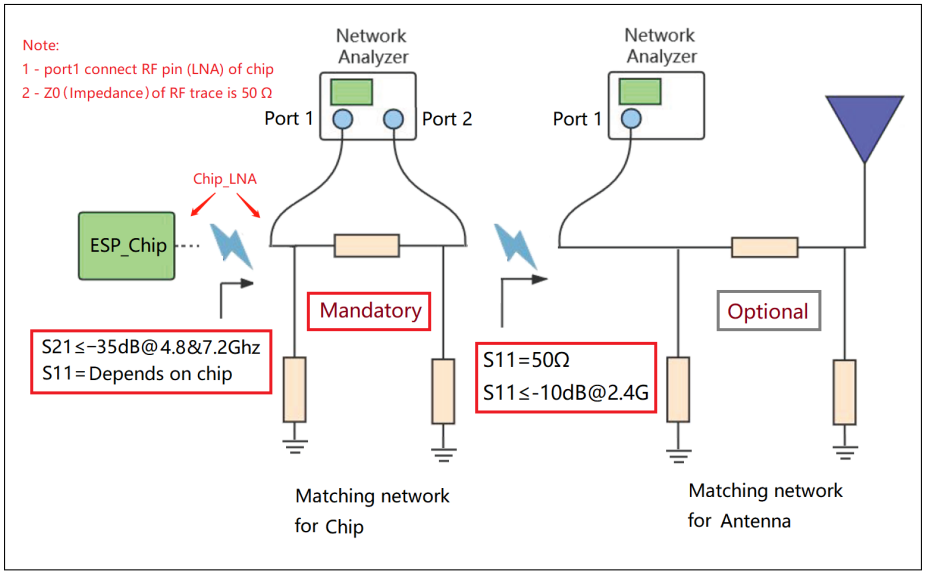

Figure 11: RF Tuning Diagram

Notice:

The matching parameters vary with board, so the ones used in our modules could not be applied directly.

2.6 UART

It is recommended to connect a 499 Ω series resistor to the U0TXD line in order to suppress the 80 MHz harmonics.

Usually UART0 is used as the serial port for download and log printing, and UART0 pins (U0TXD and U0RXD) are fixed. For instructions on download over UART0, please refer to Section 4.3.

Other UART interfaces can be used as serial ports for communication, which could be mapped to any available GPIO by software configurations. For these interfaces, it is also recommended to add a series resistor to the TX line to suppress harmonics.

When using the AT firmware, please note that the UART GPIO is already configured (refer to AT Firmware Download). It is recommended to use the default configuration.

2.7 Strapping Pins

At each startup or reset of the chip, some initial parameters should be configured, such as in which boot mode to load the chip, etc. These parameters are passed over via the strapping pins. After reset, the strapping pins operate as regular IO pins.

All the information about strapping pins is covered in *ESP32-S3 Series Datasheet* > Section *Strapping Pins*.

In this document we will mainly cover the strapping pins related to boot mode.

GPIO0 and GPIO46 control the boot mode after the reset is released. See Table 5 Chip Boot Mode Control.

Table 5: Chip Boot Mode Control

Boot Mode	GPIO0	GPIO46
Default Configuration	1 (Pull-up)	0 (Pull-down)
SPI Boot (default)	1	Any value
Download Boot	0	0
Invalid combination [1]	0	1

[1] This combination triggers unexpected behavior and should be avoided.

Regarding the timing requirements for the strapping pins, there are such parameters as *setup time* and *hold time*. For more information, see Table 6 and Figure 12.

Table 6: Description of Timing Parameters for the Strapping Pins

Parameter	Description	Min (ms)
t_{SU}	*Setup time* is the time reserved for the power rails to stabilize before the CHIP_PU pin is pulled high to activate the chip.	0
t_{H}	*Hold time* is the time reserved for the chip to read the strapping pin values after CHIP_PU is already high and before these pins start operating as regular IO pins.	3

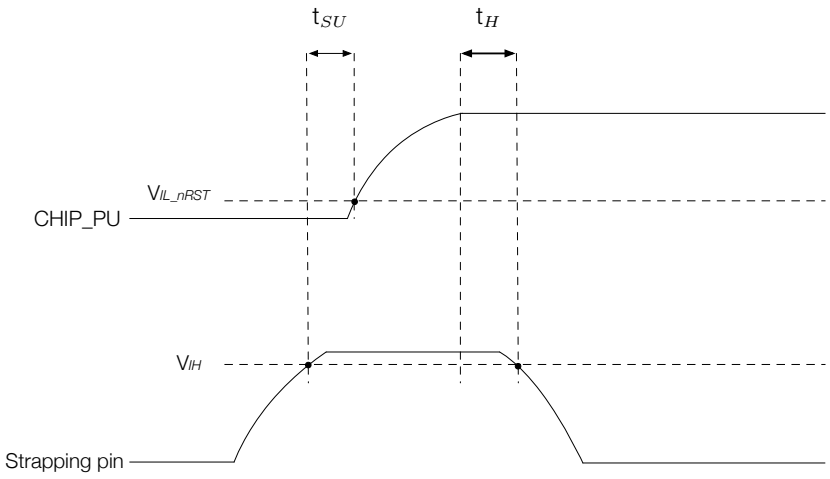

Figure 12: Visualization of Timing Parameters for the Strapping Pins

Notice:
Please do not add high-value capacitors at GPIO0, otherwise the chip not boot successfully.

2.8 GPIO

The pins of ESP32-S3 series can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations, whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to *ESP32-S3 Technical Reference Manual* > Chapter *IO MUX and GPIO Matrix*.

Some peripheral signals can only be routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to *ESP32-S3 Series Datasheet* > Section *Peripheral Pin Configurations*.

When using GPIOs:

- Pay attention to the states of strapping pins during power-up.
- Some pins will have glitches during power-up (refer to Table 8).
- Avoid using the pins already occupied by flash/PSRAM.
- When USB-OTG Download mode is enabled, some pins will have level output. See table 9 for details.
- Pay attention to their default configurations after reset (refer to Table 7). It is recommended to add a pull-up or pull-down resistor to pins in high-impedance state or enable the pull-up and pull-down during software initialization to avoid extra power consumption.
- SPICLK_N, SPICLK_P, and GPIO33 ~ GPIO37 works in the same power domain, so if octal 1.8 V flash/PSRAM is used, SPICLK_P and SPICLK_N also work in the 1.8 V power domain.
- Only GPIOs in the VDD3P3_RTC power domain can be controlled in Deep-sleep mode.

Note:
The content below is excerpted from *ESP32-S3 Series Datasheet* > Section *Pins*.

Table 7: Pin Overview

Pin No.	Pin Name	Pin Type	Pin Providing Power	Pin Settings		Pin Function Sets		
				At Reset	After Reset	IO MUX	RTC	Analog
1	LNA_IN	Analog						
2	VDD3P3	Power						
3	VDD3P3	Power						
4	CHIP_PU	Analog	VDD3P3_RTC					
5	GPIO0	IO	VDD3P3_RTC	IE, WPU	IE, WPU	**IO MUX**	RTC	
6	GPIO1	IO	VDD3P3_RTC	IE	IE	**IO MUX**	RTC	Analog
7	GPIO2	IO	VDD3P3_RTC	IE	IE	**IO MUX**	RTC	Analog
8	GPIO3	IO	VDD3P3_RTC	IE	IE	**IO MUX**	RTC	Analog
9	GPIO4	IO	VDD3P3_RTC			**IO MUX**	RTC	Analog
10	GPIO5	IO	VDD3P3_RTC			**IO MUX**	RTC	Analog
11	GPIO6	IO	VDD3P3_RTC			**IO MUX**	RTC	Analog
12	GPIO7	IO	VDD3P3_RTC			**IO MUX**	RTC	Analog
13	GPIO8	IO	VDD3P3_RTC			**IO MUX**	RTC	Analog
14	GPIO9	IO	VDD3P3_RTC		IE	**IO MUX**	RTC	Analog
15	GPIO10	IO	VDD3P3_RTC		IE	**IO MUX**	RTC	Analog
16	GPIO11	IO	VDD3P3_RTC		IE	**IO MUX**	RTC	Analog
17	GPIO12	IO	VDD3P3_RTC		IE	**IO MUX**	RTC	Analog
18	GPIO13	IO	VDD3P3_RTC		IE	**IO MUX**	RTC	Analog
19	GPIO14	IO	VDD3P3_RTC		IE	**IO MUX**	RTC	Analog
20	VDD3P3_RTC	Power						
21	XTAL_32K_P	IO	VDD3P3_RTC			**IO MUX**	RTC	Analog
22	XTAL_32K_N	IO	VDD3P3_RTC			**IO MUX**	RTC	Analog
23	GPIO17	IO	VDD3P3_RTC		IE	**IO MUX**	RTC	Analog
24	GPIO18	IO	VDD3P3_RTC		IE	**IO MUX**	RTC	Analog
25	GPIO19	IO	VDD3P3_RTC			IO MUX	RTC	**Analog**
26	GPIO20	IO	VDD3P3_RTC			IO MUX	RTC	**Analog**
27	GPIO21	IO	VDD3P3_RTC			**IO MUX**	RTC	
28	SPICS1	IO	VDD_SPI	IE, WPU	IE, WPU	**IO MUX**		
29	VDD_SPI	Power						
30	SPIHD	IO	VDD_SPI	IE, WPU	IE, WPU	**IO MUX**		
31	SPIWP	IO	VDD_SPI	IE, WPU	IE, WPU	**IO MUX**		
32	SPICS0	IO	VDD_SPI	IE, WPU	IE, WPU	**IO MUX**		
33	SPICLK	IO	VDD_SPI	IE, WPU	IE, WPU	**IO MUX**		
34	SPIQ	IO	VDD_SPI	IE, WPU	IE, WPU	**IO MUX**		
35	SPID	IO	VDD_SPI	IE, WPU	IE, WPU	**IO MUX**		
36	SPICLK_N	IO	VDD_SPI / VDD3P3_CPU	IE	IE	**IO MUX**		
37	SPICLK_P	IO	VDD_SPI / VDD3P3_CPU	IE	IE	**IO MUX**		
38	GPIO33	IO	VDD_SPI / VDD3P3_CPU		IE	**IO MUX**		
39	GPIO34	IO	VDD_SPI / VDD3P3_CPU		IE	**IO MUX**		
40	GPIO35	IO	VDD_SPI / VDD3P3_CPU		IE	**IO MUX**		
41	GPIO36	IO	VDD_SPI / VDD3P3_CPU		IE	**IO MUX**		
42	GPIO37	IO	VDD_SPI / VDD3P3_CPU		IE	**IO MUX**		
43	GPIO38	IO	VDD3P3_CPU		IE	**IO MUX**		
44	MTCK	IO	VDD3P3_CPU		IE	**IO MUX**		

Cont'd on next page

Table 7 – cont'd from previous page

Pin No.	Pin Name	Pin Type	Pin Providing Power	Pin Settings		Pin Function Sets		
				At Reset	After Reset	IO MUX	RTC	Analog
45	MTDO	IO	VDD3P3_CPU		IE	**IO MUX**		
46	VDD3P3_CPU	Power						
47	MTDI	IO	VDD3P3_CPU		IE	**IO MUX**		
48	MTMS	IO	VDD3P3_CPU		IE	**IO MUX**		
49	U0TXD	IO	VDD3P3_CPU	IE, WPU	IE, WPU	**IO MUX**		
50	U0RXD	IO	VDD3P3_CPU	IE, WPU	IE, WPU	**IO MUX**		
51	GPIO45	IO	VDD3P3_CPU	IE, WPD	IE, WPD	**IO MUX**		
52	GPIO46	IO	VDD3P3_CPU	IE, WPD	IE, WPD	**IO MUX**		
53	XTAL_N	Analog						
54	XTAL_P	Analog						
55	VDDA	Power						
56	VDDA	Power						
57	GND	Power						

Column **Pin Settings** shows predefined settings at reset and after reset with the following abbreviations:

- IE – input enabled
- WPU – internal weak pull-up resistor enabled
- WPD – internal weak pull-down resistor enabled

Some pins have glitches during power-up. See details in Table 8.

Table 8: Power-Up Glitches on Pins

Pin	Glitch[1]	Typical Time Period (μs)
GPIO1	Low-level glitch	60
GPIO2	Low-level glitch	60
GPIO3	Low-level glitch	60
GPIO4	Low-level glitch	60
GPIO5	Low-level glitch	60
GPIO6	Low-level glitch	60
GPIO7	Low-level glitch	60
GPIO8	Low-level glitch	60
GPIO9	Low-level glitch	60
GPIO10	Low-level glitch	60
GPIO11	Low-level glitch	60
GPIO12	Low-level glitch	60
GPIO13	Low-level glitch	60
GPIO14	Low-level glitch	60
XTAL_32K_P	Low-level glitch	60
XTAL_32K_N	Low-level glitch	60
GPIO17	Low-level glitch	60
GPIO18	Low-level glitch	60

	High-level glitch	60
GPIO19	Low-level glitch	60
	High-level glitch[2]	60
GPIO20	Pull-down glitch	60
	High-level glitch[2]	60

[1] Low-level glitch: the pin is at a low level output status during the time period;
High-level glitch: the pin is at a high level output status during the time period;
Pull-down glitch: the pin is at an internal weak pulled-down status during the time period;
Pull-up glitch: the pin is at an internal weak pulled-up status during the time period.

[2] GPIO19 and GPIO20 pins both have two high-level glitches during chip power-up, each lasting for about 60 μs. The total duration for the glitches and the delay are 3.2 ms and 2 ms respectively for GPIO19 and GPIO20.

2.9 ADC

Please add a 0.1 μF filter capacitor between ESP pins and ground when using the ADC function to improve accuracy. ADC1 is recommended for use.

2.10 USB

ESP32-S3 has a full-speed USB On-The-Go (OTG) peripheral with integrated transceivers. The USB peripheral is compliant with the USB 2.0 specification.

ESP32-S3 also integrates a USB Serial/JTAG controller that supports USB 2.0 full-speed device.

GPIO19 and GPIO20 can be used as D- and D + of USB respectively. It is recommended to populate zero-ohm series resistors between the mentioned pins and the USB connector. Also reserve a footprint for a capacitor to ground on each trace. Note that both components should be placed close to the ESP32-S3 chip.

ESP32-S3 also supports download functions and log message printing via USB. Please refer to Section 4.3 for download guidelines.

When USB-OTG Download mode is enabled, the chip initializes the IO pad connected to the external PHY in ROM when starts up. The status of each IO pad after initialization is as follows.

Table 9: IO Pad Status After Chip Initialization in the USB-OTG Download Mode

IO Pad	Input/Output Mode	Level Status
VP (MTMS)	INPUT	-
VM (MTDI)	INPUT	-
RCV (GPIO21)	INPUT	-
OEN (MTDO)	OUTPUT	HIGH
VPO (MTCK)	OUTPUT	LOW
VMO(GPIO38)	OUTPUT	LOW

If the USB-OTG Download mode is not needed, it is suggested to disable the USB-OTG Download mode by setting the eFuse bit EFUSE_DIS_USB_OTG_DOWNLOAD_MODE to avoid IO pad state change.

2.11 SDIO

ESP32-S3 only has one SD/MMC Host controller, which cannot be used as a slave device.

The SDIO interface can be configured to any free GPIO by software. Please add pull-up resistors to the SDIO GPIO pins, and it is recommended to reserve a series resistor on each trace.

2.12 Touch Sensor

ESP32-S3 has 14 capacitive-sensing GPIOs, i.e., GPIO1 ~ GPIO14.

The ESP32-S3 touch sensor also has a waterproof design and digital filtering feature. Note that only GPIO14 (TOUCH14) can drive the shielded electrode.

When using the touch function, it is recommended to populate a zero-ohm series resistor at the chip side to reduce the coupling noise and interference on the line, and to strengthen the ESD protection. The recommended resistance is from 470 Ω to 2 kΩ, preferably 510 Ω. The specific value depends on the actual test results of the product.

3 PCB Layout Design

This chapter introduces the key points of how to design an ESP32-S3 PCB layout using the ESP32-S3-WROOM-2 module as an example.

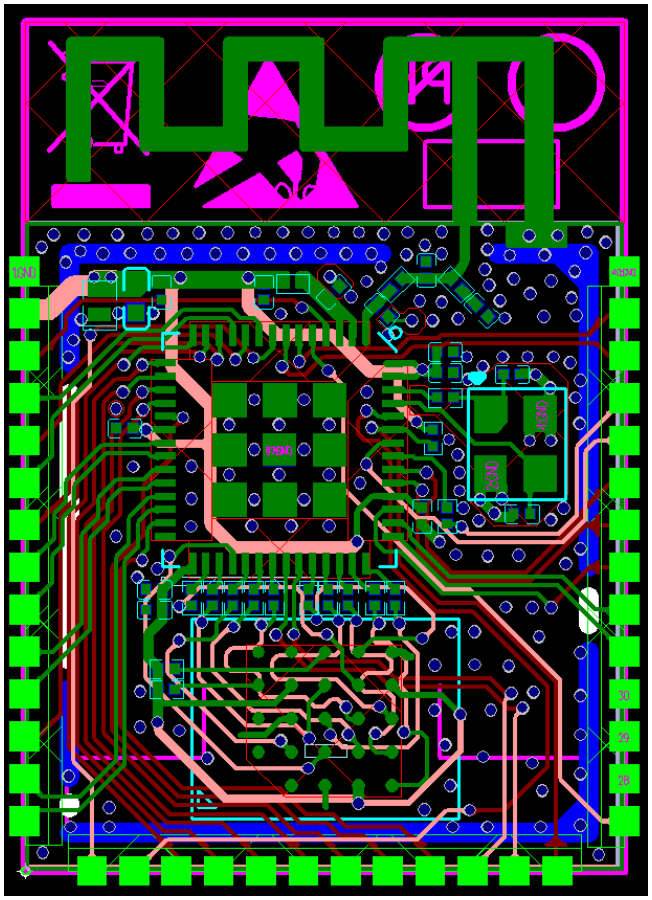

Figure 13: ESP32-S3 PCB Layout

3.1 General Principles of PCB Layout

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components.
- Layer 2 (GND): No signal traces here to ensure a complete GND plane.
- Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal. Route power traces and a few signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
- Layer 4 (BOTTOM): Route a few signal traces here. It is not recommended to place any components on this layer.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Traces and components.
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum. Please make sure there is a complete GND plane for the chip, RF, and crystal.

3.2 Positioning a Module on a Base Board

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module's antenna performance should be minimized.

It is suggested to place the module's on-board PCB antenna outside the base board, and the feed point of the antenna closest to the board. In the following example figures, positions with mark ✓are strongly recommended, while positions without a mark are not recommended.

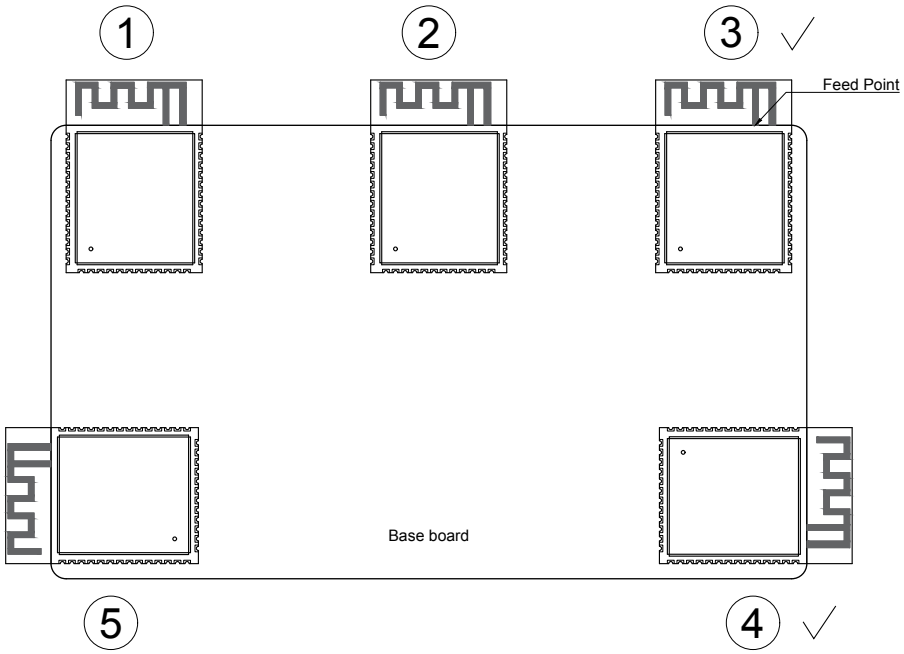

Figure 14: Placement of ESP32-S3 Modules on Base Board (Antenna Feed Point on the Right)

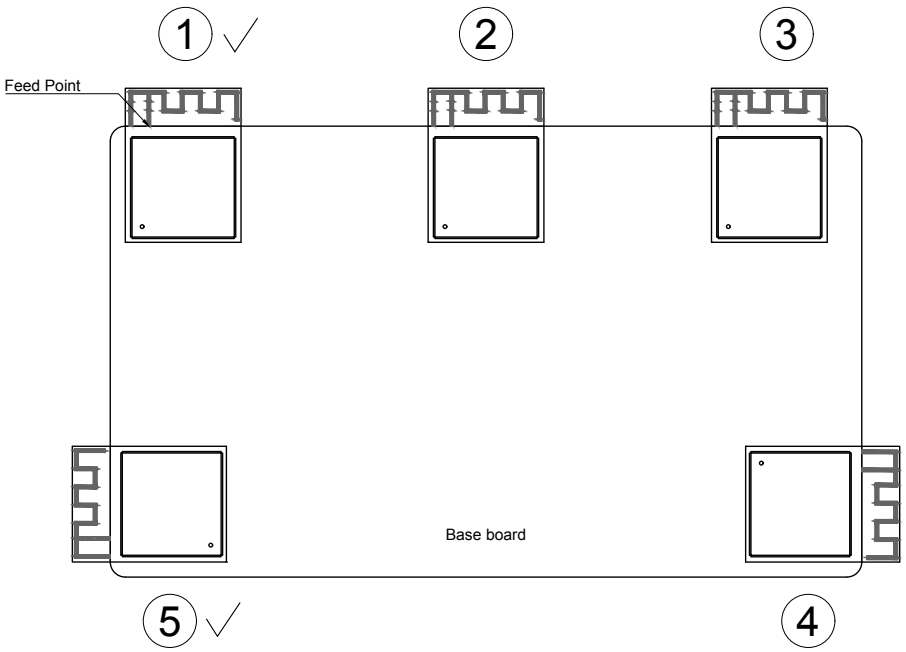

Figure 15: Placement of ESP32-S3 Modules on Base Board (Antenna Feed Point on the Left)

If PCB antenna could not be placed outside the board, please ensure a clearance of at least 15 mm around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure 16 shows the suggested clearance for modules whose antenna feed point is on the right.

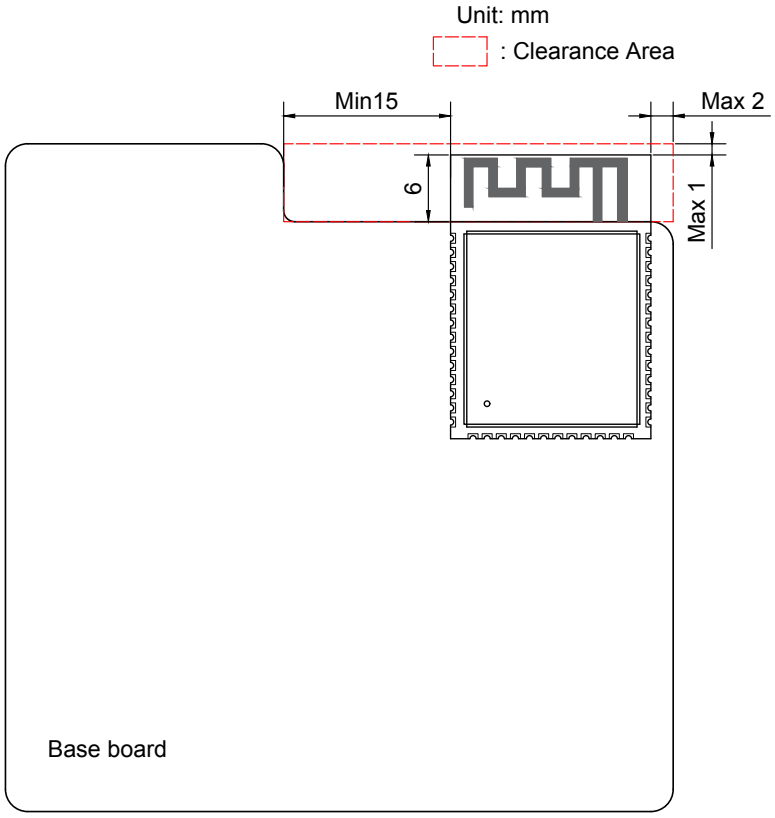

Figure 16: Keepout Zone for ESP32-S3 Module's Antenna on the Base Board

When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification.

As a conclusion, please be noted it is necessary to test the throughput and communication signal range of the whole product to ensure the product's actual RF performance.

3.3 Power Supply

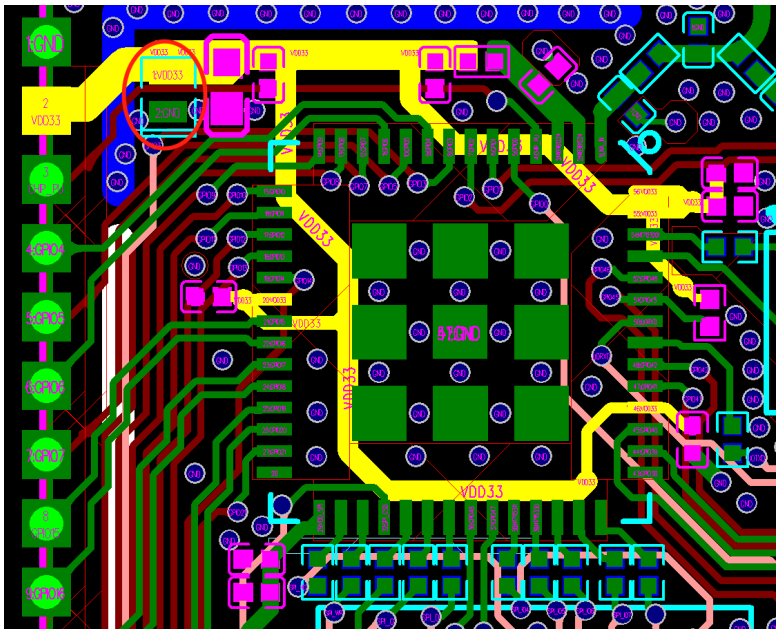

Figure 17: ESP32-S3 Power Traces in a Four-layer PCB Design

- Four-layer PCB design is preferred. The power traces should be routed on the inner third layer whenever possible. Vias are required for the power traces to go through the layers and get connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.
- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure 17. The width of the main power traces should be at least 25 mil. The width of the power traces for VDD3P3 pins should be at least 20 mil. The width of other power traces is preferably 10 mil.
- The ESD protection diode is placed next to the power port (circled in red in the top left quarter of Figure 17). The power trace should have a 10 µF capacitor on its way before entering into the chip, and a 0.1 or 1 µF capacitor could also be used in conjunction. After that, the power traces are divided into several branches using a star-shape topology, which reduces the coupling between different power pins. Note that all decoupling capacitors should be placed close to the corresponding power pin, and ground vias should be added close to the capacitor's ground pad to ensure a short return path.

> **Notice:**
> In Figure 17, the 10 μF capacitor is shared by the analog power supply VDD3P3 and the power entrance since the analog power is close to the chip power entrance. If the chip power entrance is not near the VDD3P3 pin, it is recommended to add a 10 μF capacitor to both the chip power entrance and the analog power VDD3P3, and also reserve a 1 μF capacitor if space permits.

- As shown in Figure 18, it is recommended to connect the capacitor to ground in the CLC filter circuit near VDD3P3 pins to the bottom layer through a via, and maintain a keep-out area on other layers, so as to further restrain harmonic disturbance.
- VDD3P3 analog power supply should be surrounded by ground copper. It is required to add GND isolation

between the VDD3P3 power trace and the surrounding GPIO and RF traces, and place vias whenever possible.

- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.
- If you need to add a thermal pad EPAD under the chip on the bottom of the module, it is recommended to employ a square grid on the EPAD, cover the gaps with ink, and place ground vias in the gaps, as shown in Figure 17. This can avoid chip displacement caused by tin leakage and bubbles when soldering the module EPAD to the substrate.

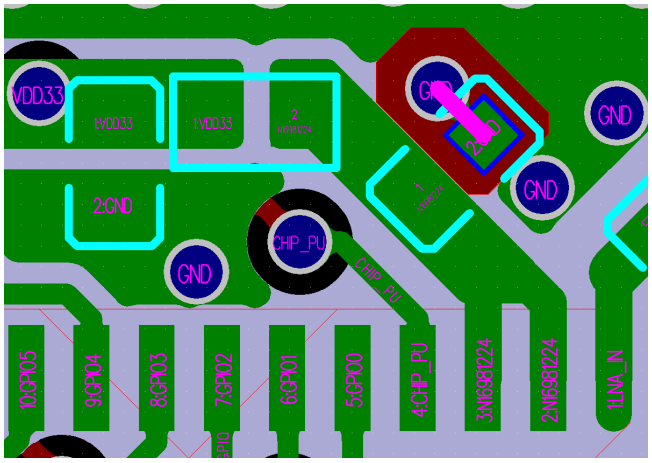

Figure 18: ESP32-S3 Analog Power Traces in a Four-layer PCB Design

3.4 Crystal

Figure 19 and Figure 20 show the reference design of the crystal. The crystal can be either connected to ground or not connected to ground in the top layer. If there is sufficient ground in the top layer, it is recommended not to connect the crystal to ground. This helps to reduce the value of parasitic capacitance and suppress temperature conduction, which can otherwise affect the frequency offset. In addition, the following should be noted:

- Ensure a complete GND plane for the RF, crystal, and chip.
- The crystal should be placed far from the clock pin to avoid the interference on the chip. **The gap should be at least 2.0 mm**. It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
- There should be no vias for the clock input and output traces, which means the traces cannot cross layers.
- Components in series to the crystal trace should be placed close to the chip side.
- The external matching capacitors should be placed on the two sides of the crystal, not connected directly to the series components, and at the end of the clock trace, to make sure the ground pad of the capacitor is close to that of the crystal.
- Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.
- As the crystal is a sensitive component, do not place any magnetic components nearby that may cause

interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

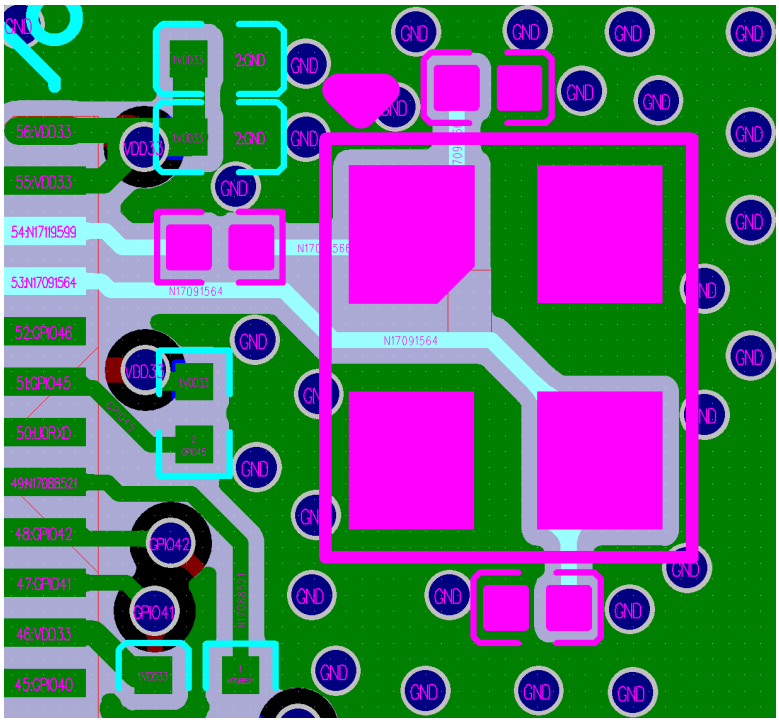

Figure 19: ESP32-S3 Crystal Layout (Connected to the Ground)

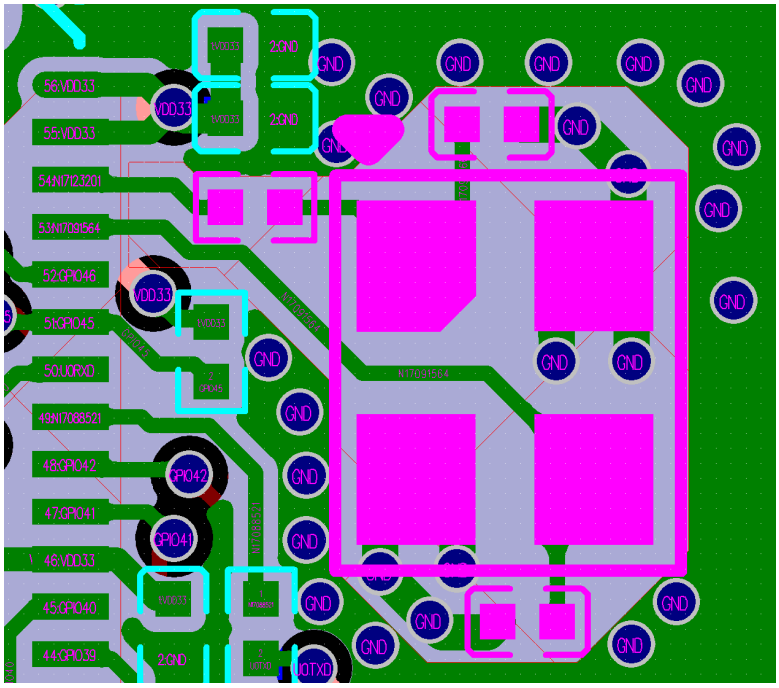

Figure 20: ESP32-S3 Crystal Layout (Not Connected to the Ground))

3.5 RF

The RF trace is routed as shown highlighted in pink in Figure 21.

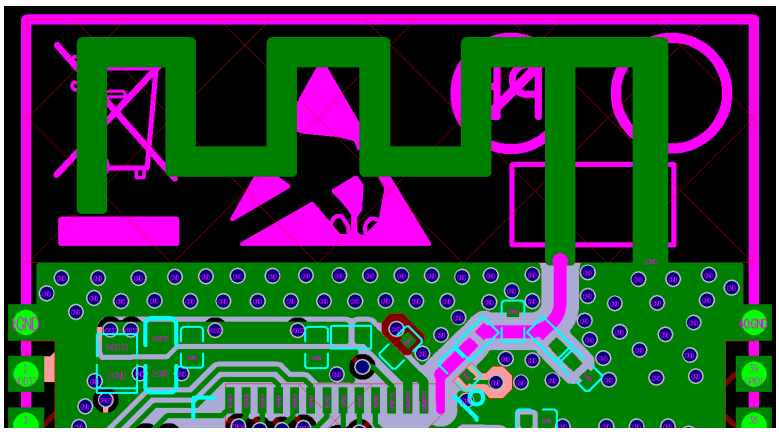

Figure 21: ESP32-S3 RF Layout in a Four-layer PCB Design

- The RF trace should have 50 Ω characteristic impedance. The reference plane is the second layer. A π-type matching circuit should be added on the RF trace and placed close to the chip, in a zigzag.
- For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown in Figure 22.

Thickness (mm)	Impedance (Ohm)	Gap (mil)	Width (mil)	Gap (mil)
-	50	12.2	12.6	12.2

Stack up	Material	Base copper (oz)	Finished Layer Thickness (mil)	DK
SM			0.4	4
L1_Top	Finished Copper 1 oz	0.33	0.8 (Min)	
PP	7628 TG150 RC50%		8	4.39
L2_Gnd		1	1.2	
Core	Core		Adjustable	4.43
L3_Power		1	1.2	
PP	7628 TG150 RC50%		8	4.39
L4_Bottom	Finished Copper 1 oz	0.33	0.8 (Min)	
SM			0.4	4

Figure 22: ESP32-S3 PCB Stack up Design

- The RF trace should have consistent width and not branch out. It should be as short as possible with dense ground vias around for inteference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- Please add a stub to ground at the ground pad of the first matching capacitor to suppress second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up, so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure 23 is the stub. Note that a stub is not required for package types above 0201.

- The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.
- There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

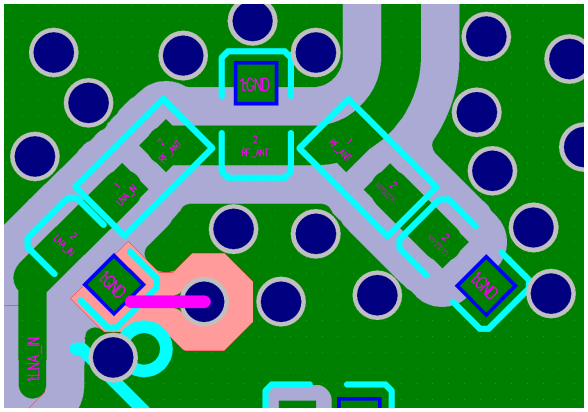

Figure 23: ESP32-S3 Stub in a Four-layer PCB Design

3.6 Flash and PSRAM

- Place the zero-ohm series resistors on the SPI lines close to the ESP32-S3 chip side.
- Route the SPI traces on the inner layer (e.g., the third layer), add ground copper and ground vias around the clock and data traces of SPI separately whenever possible.
- The 0.1 uF ground capacitor at VDD_SPI power supply can be placed close to the connected flash/PSRAM power pin.
- Octal SPI traces should have matching lengths.

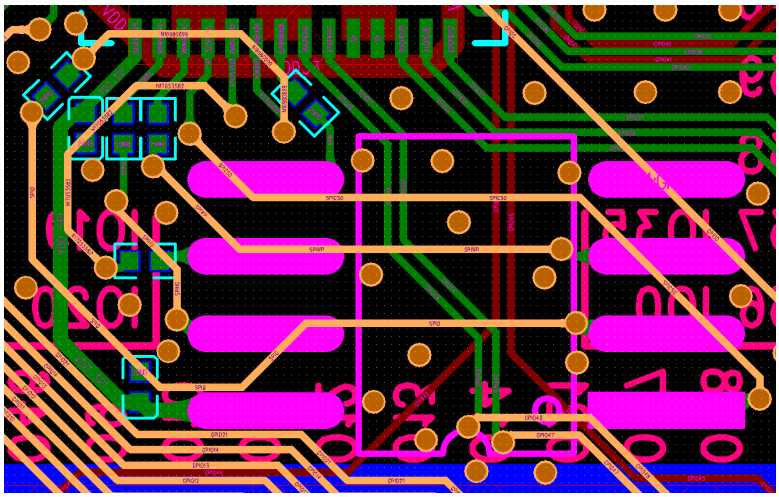

Figure 24: ESP32-S3 Quad Flash Layout

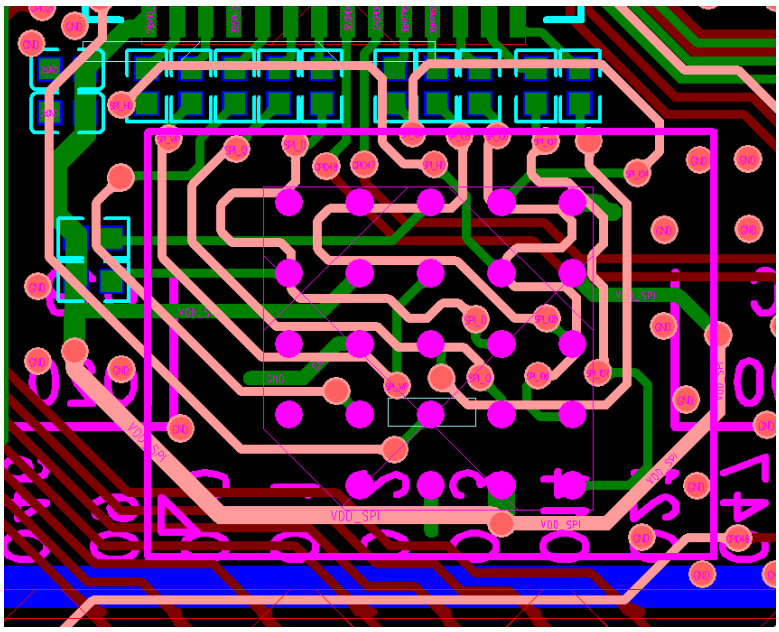

Figure 25: ESP32-S3 Octal Flash Layout

3.7 UART

- The series resistor on the U0TXD trace needs to be placed close to the ESP32-S3 chip side and away from the crystal.
- The U0TXD and U0RXD traces on the top layer should be as short as possible.
- The UART trace should be surrounded by ground copper and ground vias stitching.

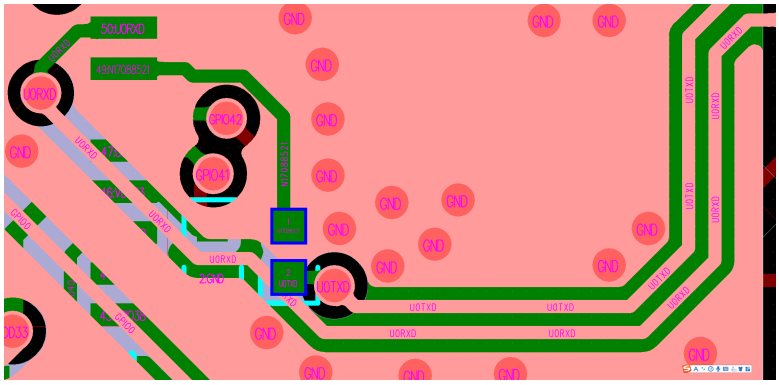

Figure 26: ESP32-S3 UART0 Layout

3.8 USB

- Place the RC circuit on the USB traces close to the ESP32-S3 chip side.
- Please use differential pairs and route them in parallel at equal lengths.
- Make sure there is a complete reference ground plane and surround the USB traces with ground copper.

3.9 SDIO

Because SDIO traces have a high speed, it is necessary to control the parasitic capacitance.

- The trace length for SDIO_CMD and SDIO_DATA0 ~ SDIO_DATA3 should be 3 mil longer or shorter than the trace length for SDIO_CLK. If necessary, use serpentine routing.
- It is better to surround the SDIO_CLK trace with ground copper. The path from SDIO GPIOs to the master SDIO interface should be as short as possible and no more than 2500 mil or even 2000 mil.
- Do not place SDIO traces across planes.

3.10 Touch Sensor

ESP32-S3 offers up to 14 capacitive IOs that detect changes in capacitance on touch sensors due to finger contact or proximity. The chip's internal capacitance detection circuit features low noise and high sensitivity. It allows to use touch pads with smaller area to implement the touch detection function. You can also use the touch panel array to detect a larger area or more test points.

Figure 27 depicts a typical touch sensor application.

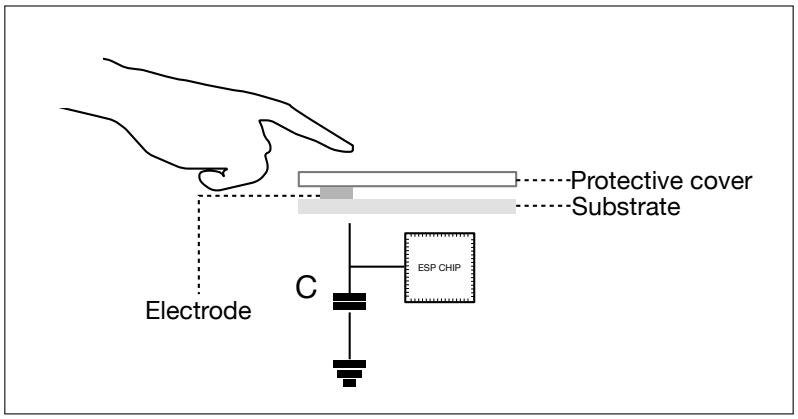

Figure 27: A Typical Touch Sensor Application

In order to prevent capacitive coupling and other electrical interference to the sensitivity of the touch sensor system, the following factors should be taken into account.

3.10.1 Electrode Pattern

The proper size and shape of an electrode improves system sensitivity. Round, oval, or shapes similar to a human fingertip are commonly applied. Large size or irregular shape might lead to incorrect responses from nearby electrodes.

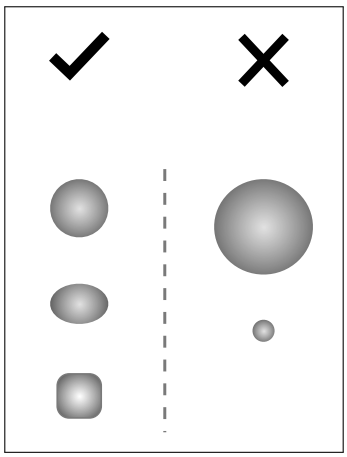

Figure 28: Electrode Pattern Requirements

Note:
The examples illustrated in Figure 28 are not of actual scale. It is suggested to use a human fingertip as reference.

3.10.2 PCB Layout

Figure 29 illustrates the general guidelines to routing traces. Specifically,

- The trace should be as short as possible and no longer than 300 mm.
- The trace width (W) can not be larger than 0.18 mm (7 mil).
- The alignment angle (R) should not be less than 90°.
- The trace-to-ground gap (S) should be in the range of 0.5 mm to 1 mm.
- The electrode diameter (D) should be in the range of 8 mm to 15 mm.
- Hatched ground should be added around the electrodes and traces.
- The traces should be isolated well and routed away from that of the antenna.

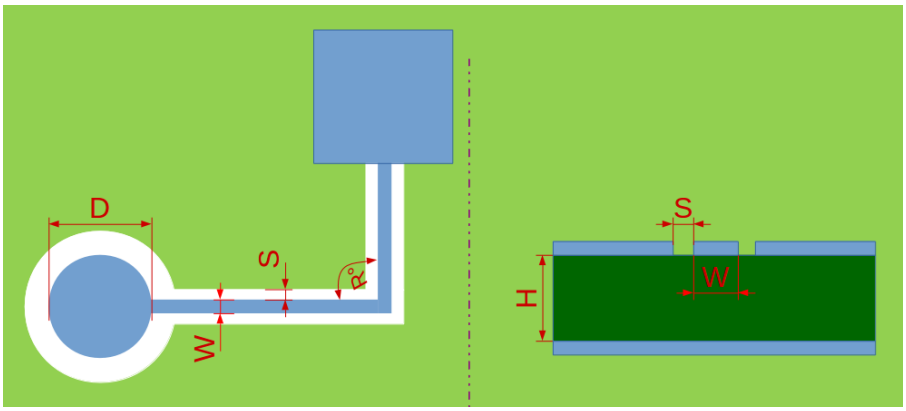

Figure 29: Sensor Track Routing Requirements

3.10.3 Waterproof and Proximity Sensing Design

ESP32-S3 touch sensor has a waterproof design and features proximity sensor function. Figure 30 shows an example layout of a waterproof and proximity sensing design.

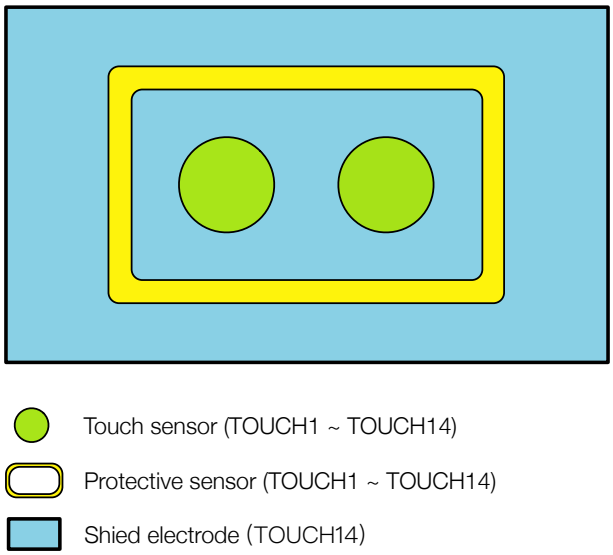

Figure 30: Shield Electrode and Protective Sensor

Note the following guidelines to better implement the waterproof and proximity sensing design:

- The recommended width of the shield electrode width is 2 cm.
- Employ a grid on the top layer with a trace width of 7 mil and a grid width of 45 mil (25% fill). The filled grid is connected to the driver shield signal.
- Employ a grid on the bottom layer with a trace width of 7 mil and a grid width of 70 mil (17% fill). The filled grid is connected to the driver shield signal.
- The protective sensor should be in a rectangle shape with curved edges and surround all other sensors.
- The recommended width of the protective sensor is 2 mm.
- The recommended gap between the protective sensor and shield sensor is 1 mm.
- The sensing distance of the proximity sensor is directly proportional to the area of the proximity sensor. However, increasing the sensing area will introduce more noise. Actual testing is needed for optimized performance.
- It is recommended that the shape of the proximity sensor is a closed loop. The recommended width is 1.5 mm.

Note:
For more details on the hardware design of ESP32-S3 touch sensor, please refer to *ESP32-S3 Touch Sensor Application Note*.

3.11 Typical Layout Problems and Solutions

3.11.1 Q: The voltage ripple is not large, but the TX performance of RF is rather poor.

Analysis:

The voltage ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP32-S3 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP32-S3 sends MCS7@11n packets, and <120 mV when ESP32-S3 sends 11m@11b packets.

Solution:

Add a 10 μF filter capacitor to the branch of the power trace (the branch powering the chip's analog power pin). The 10 μF capacitor should be as close to the analog power pin as possible for small and stable voltage ripples.

3.11.2 Q: The voltage ripple is small, but RF TX performance is poor.

Analysis:

The RF TX performance can be affected not only by voltage ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. Please see Section 3.4 for details.

3.11.3 Q: When ESP32-S3 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the π-type circuit on the RF trace, so that impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.

3.11.4 Q: TX performance is not bad, but the RX sensitivity is low.

Analysis:

Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution:

Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please see Section 3.5 for details.

4 Hardware Development

4.1 ESP32-S3 Modules

For a list of ESP32-S3 modules please check Modules section of Espressif website.

To review module reference designs please check Documentation section of Espressif website.

4.2 ESP32-S3 Development Boards

For a list of the latest designs of ESP32-S3 boards please check Development Boards section of Espressif website.

4.3 Download Guidelines

You can download firmware to ESP32-S3 either via UART or USB.

To download via UART:

1. Before the download, make sure to set the chip or module to Download Boot mode, i.e., strapping pin GPIO0 (pulled up by default) is pulled low and pin GPIO46 (pulled low by default) is left floating or pulled low. If the chip has no in-package flash or PSRAM, configure pin GPIO45 appropriately according to Table 1.
2. Power up the chip or module and check whether it has entered UART Download mode via UART0 serial port. If the log shows "waiting for download", the chip or module has entered Download Boot mode.
3. Download your firmware into flash via UART using Flash Download Tool.
4. After firmware has been downloaded, pull IO0 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the module again. The chip will read and execute the new firmware during initialization.

To download via USB:

1. Perform the download from step 3 if there is working program firmware in the flash. Otherwise, make sure to set the chip or module to Download Boot mode, i.e., strapping pin GPIO0 (pulled up by default) is pulled low and pin GPIO46 (pulled low by default) is left floating or pulled low. If the chip has no in-package flash or PSRAM, configure pin GPIO45 appropriately according to Table 1.
2. Power up the chip or module and check whether it has entered UART Download mode via USB serial port. If the log shows "waiting for download", the chip or module has entered Download Boot mode.
3. Download your firmware into flash via USB using Flash Download Tool.
4. After firmware has been downloaded, pull IO0 high or leave it floating to make sure that the chip or module enters SPI Boot mode.
5. Power up the module again. The chip will read and execute the new firmware during initialization.

Notice:

- It is advised to download the firmware only after the "waiting for download" log shows via serial ports.
- Serial tools cannot be used simultaneously with the Flash Download Tool on one com port.

- The USB auto-download will be disabled if the following conditions occur in the application, where it will be necessary to set the chip to Download Boot mode first by configuring the strapping pin.
  - USB PHY is disabled by the application;
  - USB is secondary developed for other USB functions, e.g., USB host, USB standard device;
  - USB GPIOs are configured to other peripherals, such as UART and LEDC.
- It is recommended that the user retains control of the strapping pins to avoid the USB download function not being available in case of the above scenario.

5 Related Documentation and Resources

Related Documentation

- ESP32-S3 Series Datasheet – Specifications of the ESP32-S3 hardware.
- ESP32-S3 Technical Reference Manual – Detailed information on how to use the ESP32-S3 memory and peripherals.
- ESP32-S3 Series SoC Errata – Descriptions of known errors in ESP32-S3 series of SoCs.
- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *ESP32-S3 Product/Process Change Notifications (PCN)*
  https://espressif.com/en/support/documents/pcns?keys=ESP32-S3
- *ESP32-S3 Advisories* – Information on security, bugs, compatibility, component reliability.
  https://espressif.com/en/support/documents/advisories?keys=ESP32-S3
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- ESP-IDF Programming Guide for ESP32-S3 – Extensive documentation for the ESP-IDF development framework.
- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP32-S3 Series SoCs* – Browse through all ESP32-S3 SoCs.
  https://espressif.com/en/products/socs?id=ESP32-S3
- *ESP32-S3 Series Modules* – Browse through all ESP32-S3-based modules.
  https://espressif.com/en/products/modules?id=ESP32-S3
- *ESP32-S3 Series DevKits* – Browse through all ESP32-S3-based devkits.
  https://espressif.com/en/products/devkits?id=ESP32-S3
- *ESP Product Selector* – Find an Espressif hardware product suitable for your needs by comparing or applying filters.
  https://products.espressif.com/#/product-selector?language=en

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Glossary

CLC	Capacitor-Inductor-Capacitor
DDR	Double-Data Rate
ESD	Electrostatic Discharge
LC	Inductor-Capacitor
PA	Power Amplifier
RC	Resistor-Capacitor
RTC	Real-Time Clock
SiP	System-in-Package
Zero-ohm resistor	A zero-ohm resistor is a placeholder on the circuit so that another higher ohm resistor can replace it, depending on design cases.

Revision History

Date	Version	Release Notes
2023-05-16	v1.2	• Added the following sections: – Section 2.8 *GPIO* – Section 2.11 *SDIO* – Section 3.9 *SDIO* – Section 4.3 *Download Guidelines* • Updated the following sections: – Section 2.1 *Power Supply*: Updated the notes and Figure 4 *Schematic for the Analog Power Supply Pins* – Section 2.2 *Power-up Timing and System Reset*: Adjusted the position of Figure 6 *ESP32-S3 Power-up and Reset Timing* and Table 2 *Power-up and Reset Timing* and added the note – Section 2.3 *Flash and SRAM*: Updated descriptions – Section 2.4 *Clock Source*: Updated descriptions – Section 2.5 *RF*: Updated descriptions and added Figure 11 *RF Tuning Diagram* – Section 2.6 *UART*: Added descriptions – Section 2.7 *Strapping Pins*: Updated section content – Section 2.10 *USB*: Added Table 9 *IO Pad Status After Chip Initialization in the USB-OTG Download Mode* and related descriptions – Section 3.4 *Crystal*: Added several items – Section 3.7 *UART*: Added Figure 26 *ESP32-S3 UART0 Layout* • Updated wordings throughout and other minor changes

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Date	Version	Release Notes
2022-06-02	v1.1	• Added Section 2.1.3 *RTC Power Supply* • Updated the following sections: – Section 2.1 *Power Supply* – Section 2.2 *Power-up Timing and System Reset* – Section 2.3 *Flash and SRAM* – Section 2.4.1 *External Clock Source (Compulsory)* – Section 2.7 *Strapping Pins* – Section 3.1 *General Principles of PCB Layout* – Section 3.4 *Crystal* – Section 3.6 *Flash and PSRAM* • Updated the following figures: – Figure 1 *ESP32-S3 Schematic* (including the note) – Figure 2 *ESP32-S3 Schematic for the Off-Package Octal Flash/PSRAM (1.8 V)* – Figure 13 *ESP32-S3 PCB Layout* – Figure 17 *ESP32-S3 Power Traces in a Four-layer PCB Design* – Figure 18 *ESP32-S3 Analog Power Traces in a Four-layer PCB Design* – Figure 21 *ESP32-S3 RF Layout in a Four-layer PCB Design* – Figure 23 *ESP32-S3 Stub in a Four-layer PCB Design* • Other minor updates
2021-09-30	v1.0	First release

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