**Introduction**

Hardware design guidelines give advice on how to integrate ESP8684 into other products. ESP8684 is a series of ultra-low-power Wi-Fi and Bluetooth® 5 (LE) SoCs. These guidelines will help to ensure optimal performance of your product with respect to technical accuracy and conformity to Espressif’s standards.
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1 Overview

Note:
Check the link or the QR code to make sure that you use the latest version of this document:

ESP8684 series is an ultra-low-power MCU-based SoC solution that supports 2.4 GHz Wi-Fi and Bluetooth®
Low Energy (Bluetooth LE). With its state-of-the-art power and RF performance, this SoC is an ideal choice for a
wide variety of application scenarios relating to Internet of Things (IoT), smart home, industrial automation, health
care, and consumer electronics.

At the core of this chip is a 32-bit RISC-V single-core processor that operates at up to 120 MHz. The chip
supports application development, without the need for a host MCU.

ESP8684 series provides a highly-integrated way to implement Wi-Fi and Bluetooth LE technologies using a
complete RF subsystem, including a antenna switch, RF balun, power amplifier, low noise amplifier (LNA), filter,
power management unit, calibration circuits, etc. As a result, PCB size has been greatly reduced.

With its advanced calibration circuitry, ESP8684 can dynamically adjust itself to remove external circuit
imperfections or adapt to changes in external conditions. As such, the mass production of ESP8684 series does
not require expensive and specialized Wi-Fi test equipment.

For more information about ESP8684 series, please refer to ESP8684 Series Datasheet.

Note:
Unless otherwise specified, “ESP8684” used in this document refers to the series of chips, instead of a specific chip
variant.
2 Schematic Checklist

The integrated circuitry of ESP8684 requires only 15 electrical components (resistors, capacitors, and inductors) and one crystal. The high integration of ESP8684 allows for simple peripheral circuit design. This chapter details ESP8684 schematics.

ESP8684 schematic is shown in Figure 1.

![ESP8684 Schematic](image)

The values of L3, C13, C8, L2 and C9 vary with the actual PCB board.

CHIP_EN:
H Activate chip;
L Disable chip.
This pin could not be float.

Notice: Starting from chip revision v1.1, the ESP8684 firmware supports both 26 MHz and 40 MHz crystals. For ESP8684 revision v1.0 and previous chips, please use 26 MHz instead of 40 MHz crystal. For details, you can refer to ESP8684 Series SoC Errata. You can also contact the sales team to check the chip revision.

Any basic ESP8684 circuit design may be broken down into the following major sections:
2 Schematic Checklist

- Power supply
- Power-on sequence and system reset
- Flash
- Clock source
- RF
- UART
- Strapping pins
- GPIO
- ADC

The rest of this document details the specifics of circuit design for each of these sections.

2.1 Power Supply

Details of using power supply pins can be found in Section Power Scheme in ESP8684 SeriesDatasheet.

2.1.1 Digital Power Supply

ESP864 has pin 17 VDD3P3_CPU that supplies power to CPU IO, in a voltage range of 3.0 V ~ 3.6 V. It is recommended to add an extra 0.1 \( \mu F \) filter capacitor close to this digital power supply pin.

The schematic for the digital power supply pins is shown in Figure 2.

![Figure 2: Schematic for the Digital Power Supply Pins](image)

2.1.2 Analog Power Supply

Pin 2 and 3 (both labelled VDDA3P3), pin 21 and 24 (both VDDA) are the analog power supply pins, working at 3.0 V ~ 3.6 V.

It should be noted that the sudden increase in current draw, when ESP864 is transmitting signals, may cause a power rail collapse. Therefore, it is highly recommended to add another 10 \( \mu F \) capacitor to the power trace, which can work in conjunction with the 0.1 \( \mu F \) capacitor. In addition, a CLC filter circuit needs to be added near VDDA3P3 pins so as to suppress high-frequency harmonics. The recommended rated current of the inductor is 500 mA or above. Refer to Figure 3 and place the appropriate decoupling capacitor near each analog power pin.

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If a two-layer board design is used, it is recommended to change the CLC filter circuit for pins 2 and 3 (both labelled VDDA3P3) to a CCL structure, as placing the inductance closer to the chip will yield better performance. Please refer to Figure 4 for guidance.

![Figure 3: Schematic for the Analog Power Supply Pins](image1)

The values of L3, C13, C8, L2 and C9 vary with the actual PCB board.

![Figure 4: Schematic for the Analog Power Supply Pins (Two-layer Board)](image2)

The values of L3, C13, C8, L2 and C9 vary with the actual PCB board.
2.1.3 RTC Power Supply

The pin 11 VDD3P3_RTC of ESP8684 series of chips is RTC and analog power supply pin. It is recommended to place a 0.1 \( \mu \)F decoupling capacitor near this pin in the circuit.

Please note that this power supply cannot be used as backup power.

![Figure 5: ESP8684 RTC Power Supply](image)

**Notice:**
- The recommended power supply voltage for ESP8684 is 3.3 V and the output current is no less than 500 mA.
- It is suggested to add another 10 \( \mu \)F capacitor at the power entrance. If the power entrance is close to pin 2 and pin 3, it can share the same 10 \( \mu \)F capacitor with pin 2 and pin 3.
- It is suggested to add an ESD protection diode at the power entrance.

2.2 Power-up Timing and System Reset

2.2.1 Power-up Timing

When ESP8684 uses a 3.3 V system power supply, the power rails need some time to stabilize before CHIP_EN is pulled up and the chip is enabled. Therefore, CHIP_EN needs to be powered up after the 3.3 V rails have been brought up. More details about the power-up timing can be found in Section 2.2.3.

**Notice:**
To ensure the correct power-up timing, it is advised to add an RC delay circuit at the CHIP_EN pin. The recommended setting for the RC delay circuit is usually R = 10 k\( \Omega \) and C = 1 \( \mu \)F. However, specific parameters should be adjusted based on the characteristics of the actual power supply and the power-up and reset timing sequence of the chip.

2.2.2 System Reset

CHIP_EN serves as the reset pin of ESP8684. When CHIP_EN is at low level, the reset voltage (\( V_{IL,RST} \)) should be in the range of \((-0.3 \sim 0.25 \times VDD) \) V. To avoid reboots caused by external interferences, make the CHIP_EN
trace as short as possible. Also, add a pull-up resistor as well as a capacitor to ground whenever possible. More details can be found in Section 2.2.3.

Notice:
CHIP_EN pin must not be left floating.

### 2.2.3 Power-up and Reset Timing

Figure 6 shows the power-up and reset timing of ESP8684 series of chips. Details about the parameters are listed in Table 1.

![Figure 6: ESP8684 Power-up and Reset Timing](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>t₀</td>
<td>Time reserved for the power rails of VDDA3P3, VDDPST1, VDDPST2, VDDA1 and VDDA2 to stabilize before the CHIP_EN pin is pulled high to activate the chip</td>
<td>50</td>
</tr>
<tr>
<td>t₁</td>
<td>Time reserved for CHIP_EN to stay below ( V_{IL,nRST} ) to reset the chip</td>
<td>50</td>
</tr>
</tbody>
</table>

Notice:
If the user application has one of the following scenarios:

- Slow power rise or fall, such as during battery charging or when large capacitors are present in the power supply.
- Frequent power on/off operations.
- Unstable power supply, such as in photovoltaic power generation.

Then, the RC circuit itself may not meet the timing requirements, resulting in the chip being unable to boot correctly. In this case, additional designs need to be added, such as:

- Adding an external reset chip or a watchdog chip, typically with a threshold of around 3.0 V.
- Implementing reset functionality through a button or the main controller.
2.3 Flash

ESP8684 series is embedded with 1 MB, 2 MB, or 4 MB in-package flash. The in-package flash pins are not routed out to the chip.

2.4 Clock Source

ESP8684 has two clock sources:
- External crystal oscillator clock source
- RTC clock source

2.4.1 External Clock Source (compulsory)

Starting from chip revision v1.1, the ESP8684 firmware supports 26 MHz and 40 MHz crystals.

**Notice:** Please use 26 MHz crystal instead of 40 MHz for ESP8684 revision v1.0 and previous chips. For details, you can refer to ESP8684 Series SoC Errata. You can also contact the sales team to check the chip revision.

Crystal

The circuit for the crystal is shown in Figure 7. Note that the accuracy of the selected crystal should be within ±10 ppm.

Please add a series component (resistor or inductor, see R1 in Figure 7) on the XTAL_P clock trace. Initially, please use an inductor of 24 nH to reduce the impact of high-frequency crystal harmonics on RF performance, and the value should be adjusted after an overall test.

The initial values of external capacitors C1 and C2 can be determined according to the formula:

\[ C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_{\text{stray}} \]

where the value of \( C_L \) (load capacitance) can be found in the crystal’s datasheet, and the value of \( C_{\text{stray}} \) refers to the PCB’s stray capacitance. The values of C1 and C2 need to be further adjusted after an overall test as below:

1. Select TX tone mode using the Certification and Test Tool.
2. Observe the 2.4 GHz signals with a radio communication analyzer or a spectrum analyzer and demodulate it to obtain the actual frequency offset.
3. Adjust the frequency offset to be within ±10 ppm (recommended) by adjusting the external load capacitance.
   - When the center frequency offset is positive, it means that the equivalent load capacitance is small, and the external load capacitance needs to be increased.
   - When the center frequency offset is negative, it means the equivalent load capacitance is large, and the external load capacitance needs to be reduced.
• External load capacitance at the two sides are usually equal, but in special cases, they may have slightly different values.

![Schematic for the Crystal](image)

Figure 7: Schematic for the Crystal

Notice:
• Defects in the manufacturing of crystal and oscillators (for example, large frequency deviation of more than ±10 ppm, unstable performance within operating temperature range, etc) may lead to the malfunction of ESP8684, resulting in a decrease of the RF performance.
• It is recommended that the amplitude of the crystal is greater than 500 mV.
• When Wi-Fi or Bluetooth connection fails, after ruling out software problems, you may follow the steps mentioned above to ensure that the frequency offset meets the requirements by adjusting capacitors at the two sides of the crystal.

2.4.2 RTC (optional)

ESP8684 supports an external 32.768 kHz clock signal (e.g., an oscillator) input through GPIO0 to act as the RTC clock. The amplitude of the input clock signal should be the same as the amplitude requirement of the GPIO input signal. The external RTC clock source is used to improve the timing accuracy and thus reduce the average power consumption, but will not affect the functionality.

If the RTC clock is not required, then the GPIO0 can be used as other GPIOs.

2.5 RF

The RF circuit of the ESP8684 series of chips is mainly composed of three parts, the RF traces on the PCB board, the chip matching circuit, the antenna, and the antenna matching circuit.

• For the RF traces on the PCB board, 50 Ω impedance control is required.
• The chip matching circuit must be placed close to the chip. It is recommended to use the CLCCL structure to form a bandpass filter, which is mainly used to adjust impedance points, suppress harmonics, and suppress low-frequency noise (especially in applications such as electrical lighting where the effect is significant). If there is no AC-to-DC circuit in the user application, a simpler CLC structure can be considered. The CLCCL matching circuit is shown in Figure 8.
• For the antenna and the antenna matching circuit, to ensure the radiation performance, the antenna's characteristic impedance must be around 50 Ω. Adding a CLC matching circuit near the antenna is recommended to adjust the antenna. However, if the available space is limited and the antenna impedance...
point can be guaranteed to be 50 Ω by simulation, then there is no need to add a matching circuit near the antenna.

The values of L3, C13, C8, L2 and C9 vary with the actual PCB board.

Figure 8: Schematic for RF Matching

Figure 9 shows the general process of RF tuning.

In the matching circuit, define the port near the chip as Port 1 and the port near the antenna as Port 2. S11 describes the ratio of the signal power reflected back from Port 1 to the input signal power, and S21 is used to describe the transmission loss of signal from Port 1 to Port 2. For ESP8684 series of chips, if S11 is less than or equal to -10 dB and S21 is less than or equal to -35 dB when transmitting 4.8 GHz and 7.2 GHz signals, the matching circuit can satisfy transmission requirements.

Connect the two ends of the matching circuit to the network analyzer, and test its signal reflection parameter S11 and transmission parameter S21. Adjust the values of the components in the circuit until S11 and S21 meet the requirements. If your PCB design of the chip strictly follows the PCB design stated in Chapter 3, you can refer to the value ranges in the following to debug the matching circuit:

If the components are in the 0201 SMD package size, please use a stub in the PCB design of the RF matching circuit near the chip. The recommended value ranges for the components are...
<table>
<thead>
<tr>
<th>Reference Designator</th>
<th>Recommended Value</th>
<th>Serial No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>C11</td>
<td>1.2 ~ 1.8 pF</td>
<td>GRM0335C1H1RXBA01D</td>
</tr>
<tr>
<td>L2</td>
<td>2.4 ~ 3.0 nH</td>
<td>LQP03TN2NXB02D</td>
</tr>
<tr>
<td>C12</td>
<td>1.8 ~ 1.2 pF</td>
<td>GRM0335C1H1RXBA01D</td>
</tr>
</tbody>
</table>

If the RF function is not required, the RF pin can be left floating.

If the usage or production environment is sensitive to electrostatic discharge, it is recommended to reserve ESD protection devices near the antenna.

**Notice:**
The matching parameters vary with the board, so the ones used in our modules could not be applied directly.

### 2.6 UART

It is recommended to connect a 499 Ω series resistor to the U0TXD line in order to suppress the 80 MHz harmonics.

Usually UART0 is used as the serial port for download and log printing, and UART0 pins (U0TXD and U0RXD) are fixed. For instructions on download over UART0, please refer to Section 4.3.

Other UART interfaces can be used as serial ports for communication, which could be mapped to any available GPIO by software configurations. For these interfaces, it is also recommended to add a series resistor to the TX line to suppress harmonics.

When using the AT firmware, please note that the UART GPIO is already configured (refer to AT Firmware Download). It is recommended to use the default configuration.

### 2.7 Strapping Pins

**Note:**
The content below is excerpted from Section Strapping Pins in ESP8684 Series Datasheet.

ESP8684 series has two strapping pins:
- GPIO8
- GPIO9

Software can read the values of GPIO8 and GPIO9 from GPIO_STRAPPING field in GPIO_STRAP_REG register. For register description, please refer to Section GPIO Matrix Register Summary in ESP8684 Technical Reference Manual.

During the chip's power-on reset, RTC watchdog reset, and brownout reset, the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

By default, GPIO9 is connected to the internal weak pull-up resistor. If GPIO9 is not connected or connected to an external high-impedance circuit, the latched bit value will be "1".
To change the strapping bit values, you can apply the external pull-down/pull-up resistances, or use the host MCU’s GPIOs to control the voltage level of these pins when powering on ESP8684.

After reset, the strapping pins work as normal-function pins.

Table 3 lists detailed booting configurations of the strapping pins.

### Table 3: Strapping Pins

<table>
<thead>
<tr>
<th>Booting Mode</th>
<th>Pin</th>
<th>Default</th>
<th>SPI Boot</th>
<th>Joint Download Boot</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GPIO8</td>
<td>N/A</td>
<td>Don’t care</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>GPIO9</td>
<td>Internal weak pull-up</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

#### Enabling/Disabling ROM Messages Print During Booting

<table>
<thead>
<tr>
<th>Pin</th>
<th>Default</th>
<th>Functionality</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO8</td>
<td>N/A</td>
<td>When the value of eFuse field EFUSE_UART_PRINT_CONTROL is 0 (default), print is enabled and not controlled by GPIO8. 1, if GPIO8 is 0, print is enabled; if GPIO8 is 1, it is disabled. 2, if GPIO8 is 0, print is disabled; if GPIO8 is 1, it is enabled. 3, print is disabled and not controlled by GPIO8.</td>
</tr>
</tbody>
</table>

1 The strapping combination of GPIO8 = 0 and GPIO9 = 0 is invalid and will trigger unexpected behavior.

2 Joint Download Boot mode supports UART Download Boot download method. In addition to SPI Boot and Joint Download Boot modes, ESP8684 also supports SPI Download Boot mode. For details, please see ESP8684 Technical Reference Manual > Chapter Chip Boot Control.

Figure 10 shows the setup and hold times for the strapping pins before and after the CHIP_EN signal goes high. Details about the parameters are listed in Table 4.
Table 4: Parameter Descriptions of Setup and Hold Times for the Strapping Pins

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_0 )</td>
<td>Setup time before CHIP_EN goes from low to high</td>
<td>0</td>
</tr>
<tr>
<td>( t_1 )</td>
<td>Hold time after CHIP_EN goes high</td>
<td>3</td>
</tr>
</tbody>
</table>

Notice:
Please do not add high-value capacitors at GPIO9, otherwise the chip may not boot successfully.

2.8 GPIO

Note:
The content below is excerpted from Section General Purpose Input / Output Interface (GPIO) in ESP8684 Technical Reference Manual.

The pins of ESP8684 series can be configured via IO MUX or GPIO matrix. IO MUX provides the default pin configurations, whereas the GPIO matrix is used to route signals from peripherals to GPIO pins. For more information about IO MUX and GPIO matrix, please refer to ESP8684 Technical Reference Manual > IO MUX and GPIO Matrix (GPIO, IO_MUX).

Some peripheral signals can only be routed to certain GPIO pins, while some can be routed to any available GPIO pins. For details, please refer to ESP8684 Series Datasheet > Section Peripheral Pin Configurations.

When using GPIOs,

- Please pay attention to their default configurations after reset, as shown in Table 5. It is recommended to add a pull-up or pull-down to pins in high-impedance state.
- Please be noted there are boot-up glitches for some GPIOs, as shown in 6
- Pay attention to the states of strapping pins during power-up.

Table 5: IO MUX Pin Functions

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>No.</th>
<th>Function 0</th>
<th>Function 1</th>
<th>Function 2</th>
<th>Reset</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO0</td>
<td>4</td>
<td>GPIO0</td>
<td>GPIO0</td>
<td>—</td>
<td>0</td>
<td>R, G</td>
</tr>
<tr>
<td>GPIO1</td>
<td>5</td>
<td>GPIO1</td>
<td>GPIO1</td>
<td>—</td>
<td>0</td>
<td>R, G</td>
</tr>
<tr>
<td>GPIO2</td>
<td>6</td>
<td>GPIO2</td>
<td>GPIO2</td>
<td>FSPIQ</td>
<td>1</td>
<td>R</td>
</tr>
<tr>
<td>GPIO3</td>
<td>8</td>
<td>GPIO3</td>
<td>GPIO3</td>
<td>—</td>
<td>1</td>
<td>R, G</td>
</tr>
<tr>
<td>MTMS</td>
<td>9</td>
<td>MTMS</td>
<td>GPIO4</td>
<td>FSPIHD</td>
<td>1</td>
<td>R</td>
</tr>
<tr>
<td>MTDI</td>
<td>10</td>
<td>MTDI</td>
<td>GPIO5</td>
<td>FSPIDWP</td>
<td>1</td>
<td>R, G</td>
</tr>
<tr>
<td>MTCK</td>
<td>12</td>
<td>MTCK</td>
<td>GPIO6</td>
<td>FSPICLCLK</td>
<td>1*</td>
<td>—</td>
</tr>
<tr>
<td>MTD0</td>
<td>13</td>
<td>MTD0</td>
<td>GPIO7</td>
<td>FSPID</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td>GPIO8</td>
<td>14</td>
<td>GPIO8</td>
<td>GPIO8</td>
<td>—</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td>GPIO9</td>
<td>15</td>
<td>GPIO9</td>
<td>GPIO9</td>
<td>—</td>
<td>3</td>
<td>—</td>
</tr>
<tr>
<td>GPIO10</td>
<td>16</td>
<td>GPIO10</td>
<td>GPIO10</td>
<td>FSPICS0</td>
<td>1</td>
<td>—</td>
</tr>
<tr>
<td>GPIO18</td>
<td>18</td>
<td>GPIO18</td>
<td>GPIO18</td>
<td>—</td>
<td>0</td>
<td>—</td>
</tr>
</tbody>
</table>
## Reset

The default configuration of each pin after reset:

- **0** - input disabled, in high impedance state (IE = 0)
- **1** - input enabled, in high impedance state (IE = 1)
- **2** - input enabled, pull-down resistor enabled (IE = 1, WPD = 1)
- **3** - input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
- **4** - output enabled, pull-up resistor enabled (OE = 1, WPU = 1)
- **0*** - input disabled, pull-up resistor enabled (IE = 0, WPU = 0). See details in Notes
- **1*** - When the value of eFuse bit EFUSE_DIS_PAD_JTAG is

  0, input enabled, pull-up resistor enabled (IE = 1, WPU = 1)

  1, input enabled, in high impedance state (IE = 1)

We recommend pulling high or low GPIO pins in high impedance state to avoid unnecessary power consumption. You may add pull-up and pull-down resistors in your PCB design referring to Table DC Characteristics (3.3 V, 25 °C) in [ESP8684 Series Datasheet](esp8684-series-datasheet.pdf), or enable internal pull-up and pull-down resistors during software initialization.

### Notes

- **R** - These pins have analog functions.
- **G** - These pins have glitches during power-up. See details in Table 6.

### Table 6: Power-Up Glitches on Pins

<table>
<thead>
<tr>
<th>Pin</th>
<th>Glitch</th>
<th>Typical Time Period ($\mu$s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO0</td>
<td>Low-level glitch</td>
<td>40</td>
</tr>
<tr>
<td>GPIO1</td>
<td>Low-level glitch</td>
<td>60</td>
</tr>
<tr>
<td>GPIO3</td>
<td>Low-level glitch</td>
<td>40</td>
</tr>
<tr>
<td>MTDI</td>
<td>Low-level glitch</td>
<td>60</td>
</tr>
</tbody>
</table>

$^1$ Low-level glitch: the pin is at a low level during the time period;

## 2.9 ADC

It is recommended to add a 0.1 $\mu$F filter capacitor between pins and ground when using the ADC function to improve accuracy.
3 PCB Layout Design

This chapter introduces the key points of how to design an ESP8684 PCB layout using the ESP8684-MINI-1 module as an example.

![ESP8684 PCB Layout](image)

Figure 11: ESP8684 PCB Layout

3.1 General Principles of PCB Layout

It is recommended to use a four-layer PCB design:

- Layer 1 (TOP): Signal traces and components
- Layer 2 (GND): No signal traces here to ensure a complete GND plane
- Layer 3 (POWER): GND plane should be applied to better isolate the RF and crystal parts. It is acceptable to route power traces and signal traces on this layer, provided that there is a complete GND plane under the RF and crystal.
- Layer 4 (BOTTOM): It is not recommended to place any components on this layer. It is acceptable to route signal traces on this layer when GND plane is applied.

A two-layer PCB design can also be used:

- Layer 1 (TOP): Signal traces and components
- Layer 2 (BOTTOM): Do not place any components on this layer and keep traces to a minimum to ensure a complete GND plane for the RF, crystal, and chip.
3.2 Positioning a Module on a Base Board

If module-on-board design is adopted, attention should be paid while positioning the module on the base board. The interference of the base board on the module’s antenna performance should be minimized.

It is suggested to place the module’s on-board PCB antenna outside the base board, and the feed point of the antenna closest to the board. In the following example figures, positions with mark ✓ are strongly recommended, while positions without a mark are not recommended.

![Figure 12: Placement of ESP8684 Modules on Base Board](image)

If PCB antenna could not be placed outside the board, please ensure a clearance of at least 15 mm around the antenna area (no copper, routing, or components on it), and place the feed point of the antenna closest to the board. If there is a base board under the antenna area, it is recommended to cut it off to minimize its impact on the antenna. Figure 13 shows the suggested clearance for modules whose antenna feed point is on the right.
When designing an end product, attention should be paid to the interference caused by the housing of the antenna and it is recommended to carry out RF verification.

As a conclusion, please be noted it is necessary to test the throughput and communication signal range of the whole product to ensure the product’s actual RF performance.

### 3.3 Power Supply

- Four-layer PCB design is recommended over a two-layer design. The power traces should be routed on Layer 3 whenever possible. Vias are required for the power traces to go through the layers and get
connected to the pins on the top layer. There should be at least two vias if the main power traces need to cross layers. The drill diameter on other power traces should be no smaller than the width of the power traces.

- The 3.3 V power traces, highlighted in yellow, are routed as shown in Figure 14. The width of the main power traces should be no less than 20 mil. The width of the power traces for VDDA3P3 pins should be no less than 15 mil. Recommended width of other power traces is 10 mil.

- The ESD protection diode is placed next to the power port (circled in red in the top left quarter of Figure 14). The power trace should have a 10 \( \mu \)F capacitor on its way to the chip, to be used in conjunction with a 0.1 \( \mu \)F capacitor. Then the power traces are divided into two ways from here and form a star-shape topology, thus reducing the coupling between different power pins. Note that all decoupling capacitors should be placed close to the power pin, and ground vias should be added close to the capacitor's ground pin to ensure a short return path.

- As shown in Figure 16, it is recommended to connect the capacitor to ground in the LC filter circuit near VDDA3P3 pins to the fourth layer through a via, and maintain a keep-out area on other layers.

- The power trace begins at the power entrance and reaches VDDA3P3. It is required to add GND isolation between this power trace and the GPIO traces on the left, and place vias whenever possible.

- The ground pad at the bottom of the chip should be connected to the ground plane through at least nine ground vias.

**Note:**

If you need to solder the module on another board, it is recommended to employ a four-grid EPAD on the solder mask and paste mask, cover the gaps with ink, and place ground vias in the gaps, as shown in Figure 14. This can avoid tin leakage when soldering the module.

- For the two layer PCB, please refer to the power traces in 15 to ensure a complete GND plane for the RF, crystal, and chip.
3.4 Crystal

For crystal design, please refer to 17, the crystal should be fully connected to the ground at the chip level. Please also follow the rules below:

- Ensure a complete GND plane for the RF, crystal, and chip.
- The crystal should be placed far from the clock pin to avoid the interference on the chip. **The gap should be at least 2.0 mm.** It is good practice to add high-density ground vias stitching around the clock trace for better isolation.
• There should be no vias for the clock input and output traces, which means the traces cannot cross layers.

• Components in series to the crystal trace should be placed close to the chip side.

• The external matching capacitors should be placed on the two sides of the crystal, not connected directly to the series components, and at the end of the clock trace, to make sure the ground pad of the capacitor is close to that of the crystal.

• Do not route high-frequency digital signal traces under the crystal. It is best not to route any signal trace under the crystal. The vias on the power traces on both sides of the crystal clock trace should be placed as far away from the clock trace as possible, and the two sides of the clock trace should be surrounded by grounding copper.

• As the crystal is a sensitive component, do not place any magnetic components nearby that may cause interference, for example large inductance component, and ensure that there is a clean large-area ground plane around the crystal.

![Figure 17: ESP8684 Crystal Oscillator Layout](image)

### 3.5 RF

The RF trace is routed as shown highlighted in pink in Figure 18.
The RF trace should have 50 Ω characteristic impedance. The reference plane is the second layer. A π-type matching circuit should be added on the RF trace and placed close to the chip, in a zigzag.

For designing the RF trace at 50 Ω impedance, you could refer to the PCB stack-up design shown in Figure 19.

<table>
<thead>
<tr>
<th>Thickness (mm)</th>
<th>Impedance (Ohm)</th>
<th>Gap (mil)</th>
<th>Width (mil)</th>
<th>Gap (mil)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>50</td>
<td>12.2</td>
<td>12.6</td>
<td>12.2</td>
</tr>
</tbody>
</table>

**Figure 19: ESP8684 PCB Stack up Design**

- The RF trace should have consistent width and not branch out. It should be as short as possible with dense ground vias around for interference shielding.
- The RF trace should be routed on the outer layer without vias, i.e., should not cross layers. The RF trace should be routed at a 135° angle, or with circular arcs if trace bends are required.
- Please add a stub to ground at the ground pad of the first matching capacitor to suppress second harmonics. It is preferable to keep the stub length 15 mil, and determine the stub width according to the PCB stack-up, so that the characteristic impedance of the stub is 100 Ω ± 10%. In addition, please connect the stub via to the third layer, and maintain a keep-out area on the first and second layers. The trace highlighted in Figure 20 is the stub. Note that a stub is not required for package types above 0201.
• The ground plane on the adjacent layer needs to be complete. Do not route any traces under the RF trace whenever possible.

• There should be no high-frequency signal traces routed close to the RF trace. The RF antenna should be placed away from high-frequency components, such as crystals, DDR, high-frequency clocks, etc. In addition, the USB port, USB-to-serial chip, UART signal lines (including traces, vias, test points, header pins, etc.) must be as far away from the antenna as possible. The UART signal line should be surrounded by ground copper and ground vias.

![Figure 20: ESP8684 Stub in a Four-layer PCB Design](image)

### 3.6 UART

• The series resistor on the U0TXD trace needs to be placed close to the ESP8684 chip side and away from the crystal.

• The U0TXD and U0RXD traces on the top layer should be as short as possible.

• The UART trace should be surrounded by ground copper and ground vias stitching.

![Figure 21: ESP8684 UART0](image)
3.7 Typical Layout Problems and Solutions

3.7.1 Q: The voltage ripple is not large, but the TX performance of RF is rather poor.

Analysis:

The voltage ripple has a strong impact on the RF TX performance. It should be noted that the ripple must be tested when ESP8684 is in the normal working mode. The ripple increases when the power gets high in a different mode.

Generally, the peak-to-peak value of the ripple should be <80 mV when ESP8684 sends MCS7@11n packets, and <120 mV when ESP8684 sends 11m@11b packets.

Solution:

Add a 10 \( \mu \)F filter capacitor to the branch of the power trace (the branch powering the chip's analog power pin). The 10 \( \mu \)F capacitor should be as close to the analog power pin as possible for small and stable voltage ripples.

3.7.2 Q: The voltage ripple is small, but RF TX performance is poor.

Analysis:

The RF TX performance can be affected not only by voltage ripples, but also by the crystal itself. Poor quality and big frequency offsets of the crystal decrease the RF TX performance. The crystal clock may be corrupted by other interfering signals, such as high-speed output or input signals. In addition, high-frequency signal traces, such as the SDIO traces and UART traces under the crystal, could also result in the malfunction of the crystal. Besides, sensitive components or radiating components, such as inductors and antennas, may also decrease the RF performance.

Solution:

This problem is caused by improper layout and can be solved by re-layout. Please see Section 3.4 for details.

3.7.3 Q: When ESP8684 sends data packages, the power value is much higher or lower than the target power value, and the EVM is relatively poor.

Analysis:

The disparity between the tested value and the target value may be due to signal reflection caused by the impedance mismatch on the transmission line connecting the RF pin and the antenna. Besides, the impedance mismatch will affect the working state of the internal PA, making the PA prematurely access the saturated region in an abnormal way. The EVM becomes poor as the signal distortion happens.

Solution:

Match the antenna's impedance with the \( \pi \)-type circuit on the RF trace, so that the impedance of the antenna as seen from the RF pin matches closely with that of the chip. This reduces reflections to the minimum.
3.7.4 Q: TX performance is not bad, but the RX sensitivity is low.

Analysis:

Good TX performance indicates proper RF impedance matching. Poor RX sensitivity may result from external coupling to the antenna. For instance, the crystal signal harmonics could couple to the antenna. If the TX and RX traces of UART cross over with RF trace, they will affect the RX performance, as well. If there are many high-frequency interference sources on the board, signal integrity should be considered.

Solution:

Keep the antenna away from crystals. Do not route high-frequency signal traces close to the RF trace. Please see Section 3.5 for details.
4 Hardware Development

4.1 ESP8684 Modules

For a list of ESP8684 modules please check [Modules](#) section of Espressif website.

To review module reference designs please check [Documentation](#) section of Espressif website.

4.2 ESP8684 Development Boards

For a list of the latest designs of ESP8684 boards please check [Development Boards](#) section of Espressif website.

4.3 Download Guidelines

You can download firmware to ESP8684 either via UART.

To download via UART:

1. Before the download, make sure to set the chip or module to Joint Download Boot mode, i.e., strapping pin GPIO8 (floating by default) is pulled high and pin GPIO9 (pulled up by default) is pulled low.

2. Power up the chip or module and check the log via UART0 serial port. If the log shows “waiting for download”, the chip or module has entered Joint Download Boot mode.

3. Download your firmware into flash via UART using Flash Download Tool.

4. After firmware has been downloaded, pull GPIO9 high or leave it floating to make sure that the chip or module enters SPI Boot mode.

5. Power up the module again. The chip will read and execute the new firmware during initialization.

**Notice:**

- Before downloading the firmware, it is advised to check if the chip has entered Download Boot mode or not via serial tools.

- Serial tools cannot be used simultaneously with the Flash Download Tool.
5 Related Documentation and Resources

Related Documentation

- **ESP8684 Series Datasheet** – Specifications of the ESP8684 hardware.
- **ESP8684 Technical Reference Manual** – Detailed information on how to use the ESP8684 memory and peripherals.
- **ESP8684 Series SoC Errata** – Descriptions of known errors in ESP8684 series of SoCs.
- **Certificates**
- **ESP8684 Product/Process Change Notifications (PCN)**
- **Documentation Updates and Update Notification Subscription**

Developer Zone

- **ESP-IDF and other development frameworks on GitHub.**
  https://github.com/espressif
- **ESP32 BBS Forum** – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- **The ESP Journal** – Best Practices, Articles, and Notes from Espressif folks.
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- **ESP8684 Series Modules** – Browse through all ESP8684-based modules.
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  https://espressif.com/en/contact-us/sales-questions
### Glossary

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<th>Description</th>
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<tr>
<td>CLC</td>
<td>Capacitor-Inductor-Capacitor</td>
</tr>
<tr>
<td>DDR</td>
<td>Double-Data Rate</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
</tr>
<tr>
<td>LC</td>
<td>Inductor-Capacitor</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>RC</td>
<td>Resistor-Capacitor</td>
</tr>
<tr>
<td>RTC</td>
<td>Real-Time Clock</td>
</tr>
<tr>
<td>SiP</td>
<td>System-in-Package</td>
</tr>
<tr>
<td>Zero-ohm resistor</td>
<td>A zero-ohm resistor is a placeholder on the circuit so that another higher ohm resistor can replace it, depending on design cases.</td>
</tr>
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## Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Release Notes</th>
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<tr>
<td>2023-09-21</td>
<td>v1.5</td>
<td>• Added support for 40 MHz crystal</td>
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<tr>
<td></td>
<td></td>
<td>• Updated Power Supply and added principles for two layer PCB design.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Updated RF</td>
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<tr>
<td>2023-01-04</td>
<td>v1.4</td>
<td>• Updated RTC Power Supply</td>
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<tr>
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<td></td>
<td>• Updated Flash</td>
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<td></td>
<td></td>
<td>• Updated External Clock Source (compulsory)</td>
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<tr>
<td>2022-10-13</td>
<td>v1.3</td>
<td>Updated RF</td>
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<tr>
<td>2022-07-01</td>
<td>v1.2</td>
<td>• Added 26 MHz crystal</td>
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<td>• Updated ESP8684 Schematic</td>
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<td>• Updated Schematic for the Analog Power Supply Pins</td>
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<tr>
<td></td>
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<td>• Updated Schematic for the Crystal</td>
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<tr>
<td>2022-05-20</td>
<td>v1.1</td>
<td>Added section RTC (optional)</td>
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<tr>
<td>2022-05-05</td>
<td>v1.0</td>
<td>First release</td>
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<td>2022-01-10</td>
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