ESP32 Phy Init Bin

Parameter Configuration Guide

Version 1.0
Espressif Systems

About This Guide

This guide provides the parameter configuration for ***ESP32 phy init bin***.

Release Notes

Date	Version	Release notes
2018.12	V1.0	Initial release

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1. Structure of *ESP32 Phy Init Bin*

Table 1-1 outlines the structure of ***ESP32 phy init bin***:

Table 1-1. Structure of ESP32 Phy Init Bin

Name	Size
parity bits 1 (start bit)	8 bytes
phy init data	128 bytes
parity bits 2 (stop bit)	8 bytes

2. Version of *ESP32 Phy Init Bin*

The version information of ***ESP32 phy init bin*** is stored in byte [0] of ***phy init data***.

For example, ***ESP32_esp_data_bin_v05.bin*** represents Version 05, which is stored in byte [0] as '0x5'.

Table 2-1. Version of ESP32 Phy Init Bin

Location in *phy init bin*	Location in *phy init data*	Parameter Name	Default Value	Description
8	0	***Init_bin_version***	5	***phy init bin*** version

3. Six Levels of TX Power

TX power can be switched between six levels. The indexes for the six levels are the numbers from 0 to 5 at the end of the parameter names. For example, the index for ***txpwr_qdb_0*** is 0, representing the maximum TX power. From ***txpwr_qdb_0*** to ***txpwr_qdb_5,*** the TX power decreases progressively.

See Table 3-1:

Table 3-1. Six Levels of TX Power

Location in *phy init bin*	Location in *phy init data*	Parameter Name	Default Value	Measurement Unit	Actual TX Power
52	44	***txpwr_qdb_0***	78	0.25 dB	19.5 dBm
53	45	***txpwr_qdb_1***	76	0.25 dB	19 dBm
54	46	***txpwr_qdb_2***	74	0.25 dB	18.5 dBm
55	47	***txpwr_qdb_3***	68	0.25 dB	17 dBm
56	48	***txpwr_qdb_4***	60	0.25 dB	15 dBm
57	49	***txpwr_qdb_5***	52	0.25 dB	13 dBm

4. TX Power for Various Data Rates

You can choose from any of the six TX power levels for different data rates and the default value means the index of TX power, see Table 4-1:

Table 4-1. TX Power for Various Date Rates

Location in *phy init bin*	Location in *phy init data*	Parameter name	Data rate/mode	Default value	Description
58	50	***txpwr_index_0***	MCS0, 6 Mbit/s, 9 Mbit/s	1	Select ***txpwr_qdb_1***
59	51	***txpwr_index_1***	MCS1, 12 Mbit/s	1	Select ***txpwr_qdb_1***
60	52	***txpwr_index_2***	MCS2, 18 Mbit/s	1	Select ***txpwr_qdb_1***
61	53	***txpwr_index_3***	MCS3, 24 Mbit/s	2	Select ***txpwr_qdb_2***
62	54	***txpwr_index_4***	MCS4, 36 Mbit/s	2	Select ***txpwr_qdb_2***
63	55	***txpwr_index_5***	MCS5, 48 Mbit/s	3	Select ***txpwr_qdb_3***
64	56	***txpwr_index_6***	MCS6, 54 Mbit/s	4	Select ***txpwr_qdb_4***
65	57	***txpwr_index_7***	MCS7	5	Select ***txpwr_qdb_5***
66	58	***txpwr_index_11b_en***	802.11b	1	0: use ***txpwr_index_0*** to set TX Power for 802.11b 1: use byte [59], [60] to set TX Power for 802.11b
67	59	***txpwr_index_11b_0***	1 Mbit/s, 2 Mbit/s	0	Select ***txpwr_qdb_0***
68	60	***txpwr_index_11b_1***	5.5 Mbit/s, 11 Mbit/s	0	Select ***txpwr_qdb_0***

5. TX Power Limits

The TX power limits have been set mainly to limit the maximum output powers for different channels and modes in order to conform to the certification test results.

The setting is applicable to PHY version 3910 or above.

5.1. Value Range of the TX Power Limits

The TX power limits are set against the six levels. The value range of the limits is [0:10], which includes the values presented in Table 5-1.

Table 5-1. Values of the TX Power Limits

Value	TX Power Limit (Unit: dBm)
0	***txpwr_qdb_0*** / 4
1	***txpwr_qdb_1*** / 4
2	***txpwr_qdb_2*** / 4
3	***txpwr_qdb_3*** / 4
4	***txpwr_qdb_4*** / 4
5	***txpwr_qdb_5*** / 4
6	(***txpwr_qdb_5*** / 4) - 1
7	(***txpwr_qdb_5*** / 4) - 2
8	(***txpwr_qdb_5*** / 4) - 3
9	(***txpwr_qdb_5*** / 4) - 4
10	(***txpwr_qdb_5*** / 4) - 5

5.2. Parameters of the TX Power Limits

Parameters of the TX power limits are specified in Table 5-2.

1. The maximum TX powers for 802.11b/g/n mode channels 1~14 are configurable for the 20 MHz bandwidth.

   Example 1: the parameter ***mpwr_cbw20_chan1*** can be configured as follows:

   - bit[3:0] set TX power limit for 802.11g/n mode channel 1, range [0:10].
   - bit[7:4] set TX power limit for 802.11b mode channel 1, range [0:10].

> 📖 ***Note 1:***
>
> ***mpwr_cbw20_chan2*** *to* ***mpwr_cbw20_chan14*** *are configured the same as* ***mpwr_cbw20_chan1*** *in corresponding mode and channel.*

2. The maximum TX powers for 802.11n mode channels 3~11 are configurable for the 40 MHz bandwidth

   Example 2: the parameter ***mpwr_cbw40_chan3_4*** can be configured as follows:

   - bit[3:0] set TX power limit for 802.11n mode channel 3, range [0:10].
   - bit[7:4] set TX power limit for 802.11n mode channel 4, range [0:10].

> 📖 ***Note 2:***
>
> ***mpwr_cbw40_chan5_6*** *to* ***mpwr_cbw40_chan11*** *are configured the same as* ***mpwr_cbw40_chan3_4*** *in corresponding mode and channel.*

Table 5-2. Parameters of the TX Power Limits

Location in *phy init bin*	Location in *phy init data*	Parameter name	Default value	Description
69	61	***fcc_enable***	0	0: disable byte [62] - [80] 1: reserved for old version 2: enable byte [62] - [80] to set maximum TX power
70	62	***mpwr_cbw20_chan1***	0	Please refer to Example 1
71	63	***mpwr_cbw20_chan2***	0	Please refer to Note 1
72	64	***mpwr_cbw20_chan3***	0	Please refer to Note 1
73	65	***mpwr_cbw20_chan4***	0	Please refer to Note 1
74	66	***mpwr_cbw20_chan5***	0	Please refer to Note 1
75	67	***mpwr_cbw20_chan6***	0	Please refer to Note 1
76	68	***mpwr_cbw20_chan7***	0	Please refer to Note 1
77	69	***mpwr_cbw20_chan8***	0	Please refer to Note 1
78	70	***mpwr_cbw20_chan9***	0	Please refer to Note 1
79	71	***mpwr_cbw20_chan10***	0	Please refer to Note 1
80	72	***mpwr_cbw20_chan11***	0	Please refer to Note 1
81	73	***mpwr_cbw20_chan12***	0	Please refer to Note 1
82	74	***mpwr_cbw20_chan13***	0	Please refer to Note 1

83	75	***mpwr_cbw20_chan14***	0	Please refer to Note 1
84	76	***mpwr_cbw40_chan3_4***	0	Please refer to Example 2
85	77	***mpwr_cbw40_chan5_6***	0	Please refer to Note 2
86	78	***mpwr_cbw40_chan7_8***	0	Please refer to Note 2
87	79	***mpwr_cbw40_chan9_10***	0	Please refer to Note 2
88	80	***mpwr_cbw40_chan11***	0	Please refer to Note 2

6. CRC8 Check

The CRC8 checksum for bytes from byte [0] to [126] is stored in byte [127] of ***phy init data***.

> ⚠ ***Note:***
>
> *If you need to have **phy init data** parameters adjusted, please contact us。*

Espressif IoT Team

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